USBXpress™ ファミリ CP2102N データシート

USBXpress ファミリの CP2102N デバイスは、ファームウェアの複雑さを解消し、開発時間を短縮することで、USB をアプリケーションに迅速に追加できるよう設計されています。

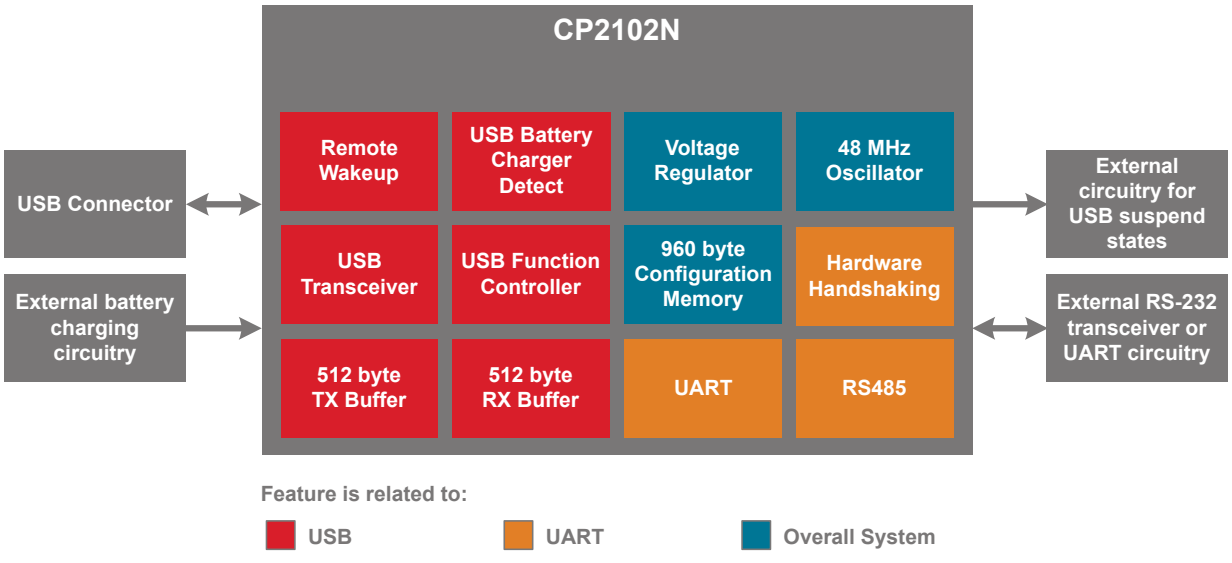
高度に統合されたこれらの USB/UART ブリッジ・コントローラを使用することで、最小限のコンポーネントと PCB スペースを使用して、RS-232 設計を USB に簡単にアップデートすることができます。CP2102N は、 3 mm x 3 mm の小さなパッケージに USB 2.0 フルスピード機能コントローラ、USB トランシーバ、発振器、および汎用非同期レシーバ/トランスミッタを備えています。その他の外部 USB コンポーネントは不要です。簡易な GUI ベースのコンフィギュレータを使用して、カスタマイズと構成のすべてのオプションを選択できます。複雑なファームウェアとドライバ開発の必要性をなくすことにより、CP2102N デバイスは、最小限の開発作業で迅速な USB 接続性を実現します。

CP2102N デバイスは、以下を含む広範なアプリケーションに理想的です。

- POS 端末
- USB ドングル
- ゲーム・コントローラ
- 医療機器
- データ・ロガ

主な機能

- ファームウェア開発が不要
- 簡易な GUI ベースのコンフィギュレータ
- 統合された USB トランシーバ、外部抵抗不要
- 統合されたクロック、外部水晶不要
- USB 2.0 フルスピード互換
- データ転送速度最大 3 Mbaud
- USB バッテリ・チャージャ検出 (USB BCS 1.2 仕様)
- 中断されたホストのスリープを解除するためのリモート・ウェイクアップ
- 低動作電流: 9.5 mA
- ロイヤリティなしの仮想 COM ポート・ドライバ



第 1 章 機能リストと注文情報

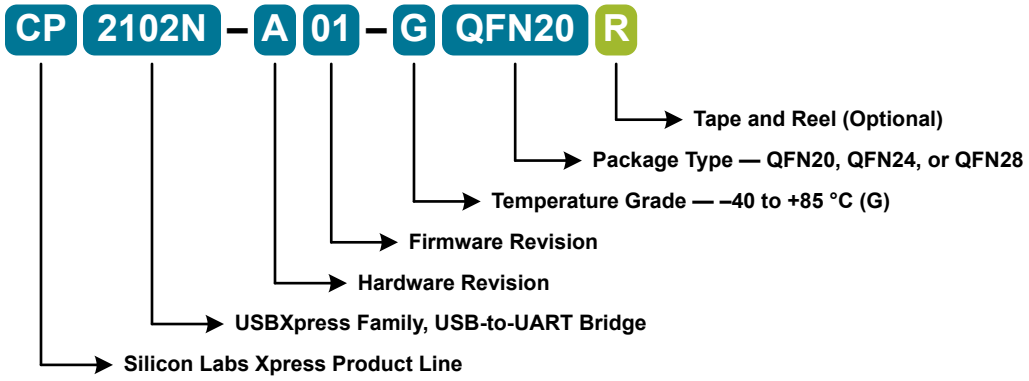


図 1.1. CP2102N 部品番号

CP2102N デバイスには以下の特徴があります。

- **シングルチップ USB/UART データ転送**
  - 統合された USB トランシーバ、外部抵抗不要
  - 統合されたクロック、外部水晶不要
  - ベンダー ID、製品 ID、シリアル番号、電源記述子、リリース番号、および商品の説明文字列のための内部 960 バイト・プログラム可能 ROM
  - オンチップ・パワー・オン・リセット (POR) 回路
  - オンチップ電圧レギュレータ – 3.3 V 出力
  - CP2101/2/9 対応のピン（QFN28 パッケージ）
  - CP2104 対応のピン（QFN24 パッケージ）
- **USB 機能コントローラ**
  - USB 仕様 2.0 準拠、フルスピード（12Mbps）
  - サスペンド・ピンを介して USB サスペンド状態をサポート
  - USB バッテリ・チャージャ検出（USB BCS 1.2 仕様）
  - 中断されたホストのスリープを解除するためのリモート・ウェイクアップ
- **3.0 ～ 3.6 V または 3.0 ～ 5.25 V の単一電源**
- **汎用非同期レシーバ/トランスミッタ（UART）**
  - すべてのハンドシェイクおよびモデムのインターフェイス信号
  - サポートされるデータ形式
    - データ・ビット – 5、6、7、8
    - ストップ・ビット – 1、1.5、2
    - パリティ – 奇数、偶数、マーク、スペース、パリティなし
  - ボーレート：300 baud ～ 3 Mbaud
  - 512 バイト受信バッファ
  - 512 バイト送信バッファ
  - ハードウェアまたは Xon/Xoff ハンドシェイク対応
- **仮想 COM ポート・デバイス・ドライバ**
  - 既存の COM ポート・アプリケーションで動作
  - Windows、Mac、および Linux でサポート
  - ロイヤリティなしの配布ライセンス
- **ダイレクト・ドライバ・サポート**
  - ロイヤリティなしの配布ライセンス

表 1.1. Product Selection Guide

Ordering Part Number	GPIOs	Battery Charger Detect	Separate VIO and VDD Pins	Pb-free (RoHS Compliant)	Temperature Range	Package
CP2102N-A02-GQFN28	7	Yes	—	Yes	-40 to +85 °C	QFN28
CP2102N-A02-GQFN24	4	—	Yes	Yes	-40 to +85 °C	QFN24
CP2102N-A02-GQFN20	4	—	—	Yes	-40 to +85 °C	QFN20

Note:
1. Devices with the same ordering part number may have different types of pin 1 indicators. However, all of these variants can use the same landing diagram as long as the recommended landing diagram instructions are followed.

Table of Contents

2. Typical Connection Diagrams

2.1 Power

In all cases, a 1 kΩ pull-up on the RSTb pin is recommended. This pull-up should be tied to VIO on devices that have it. On devices where VIO is connected to VDD or devices that do not have VIO, this pull-up should be tied to VDD. The RSTb pin will be driven low during power-on and power failure reset events.

The figure below shows a typical connection diagram for the power pins of the CP2102N devices when the internal regulator is used and USB is connected (bus-powered).

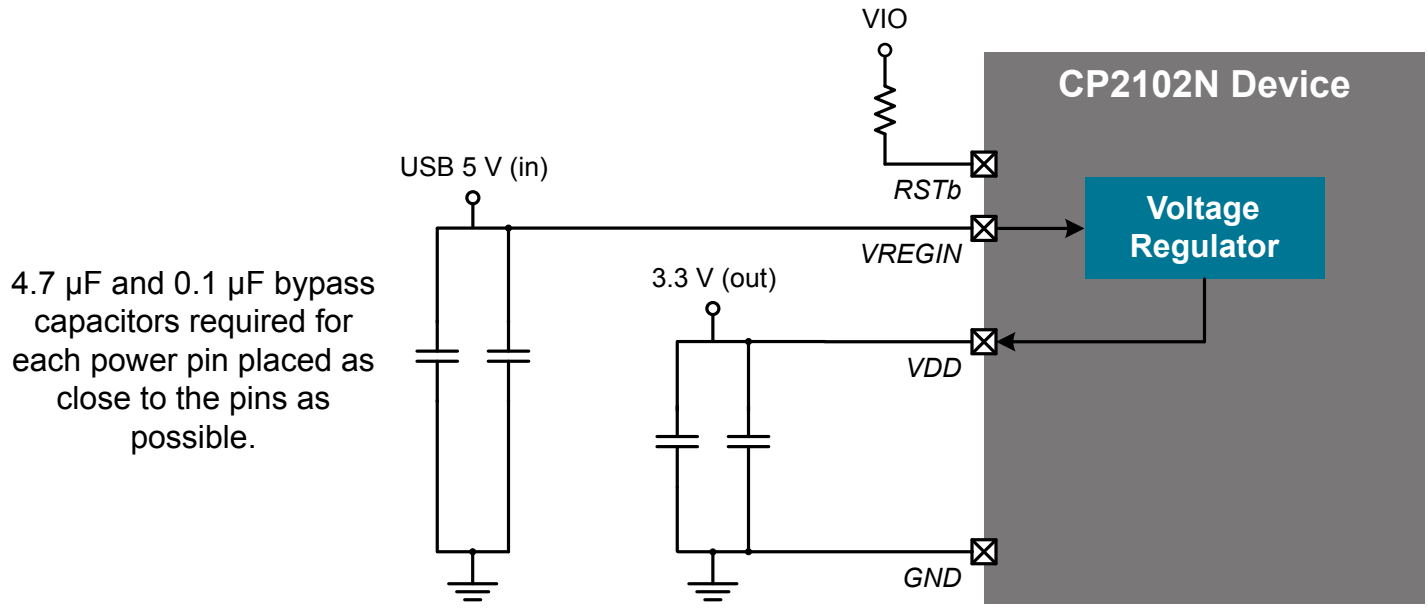


Figure 2.1. Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered)

The figure below shows a typical connection diagram for the power pins of the CP2102N devices when the internal regulator is used and USB is connected (self-powered).

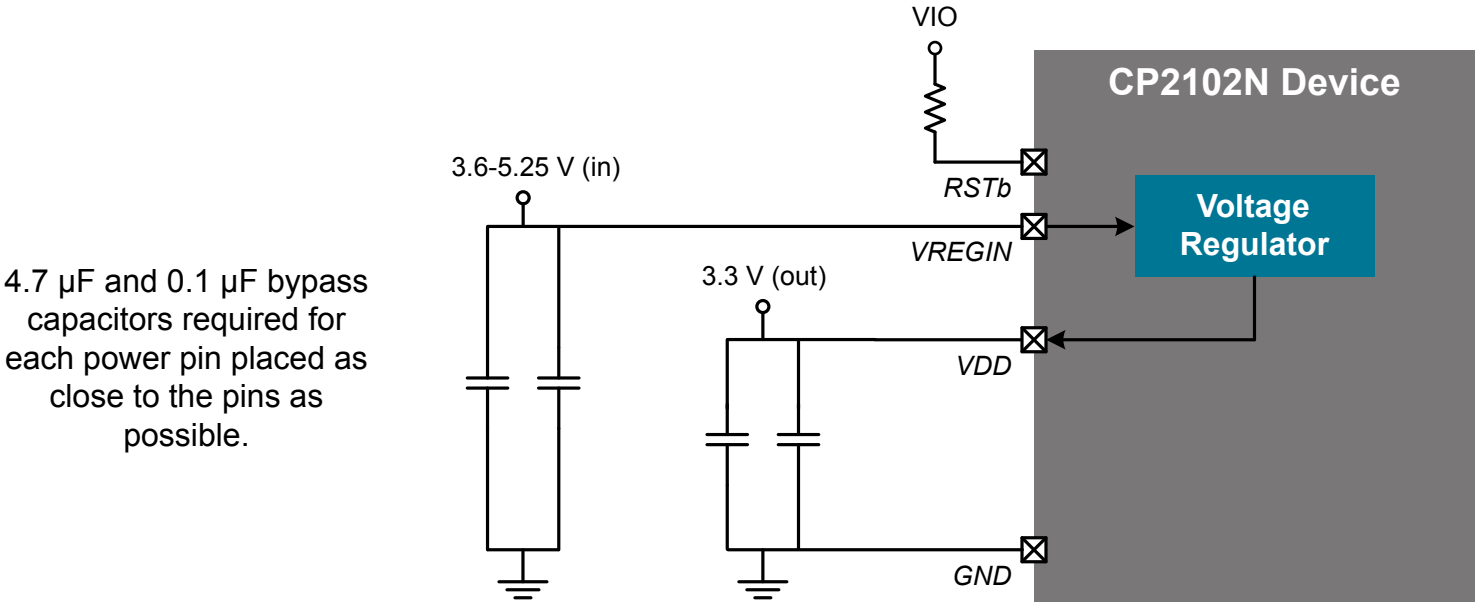


Figure 2.2. Connection Diagram with Voltage Regulator Used and USB Connected (Self-Powered)

The figure below shows a typical connection diagram for the power pins of the CP2102N devices when the internal 5 V-to-3.3 V regulator is not used.

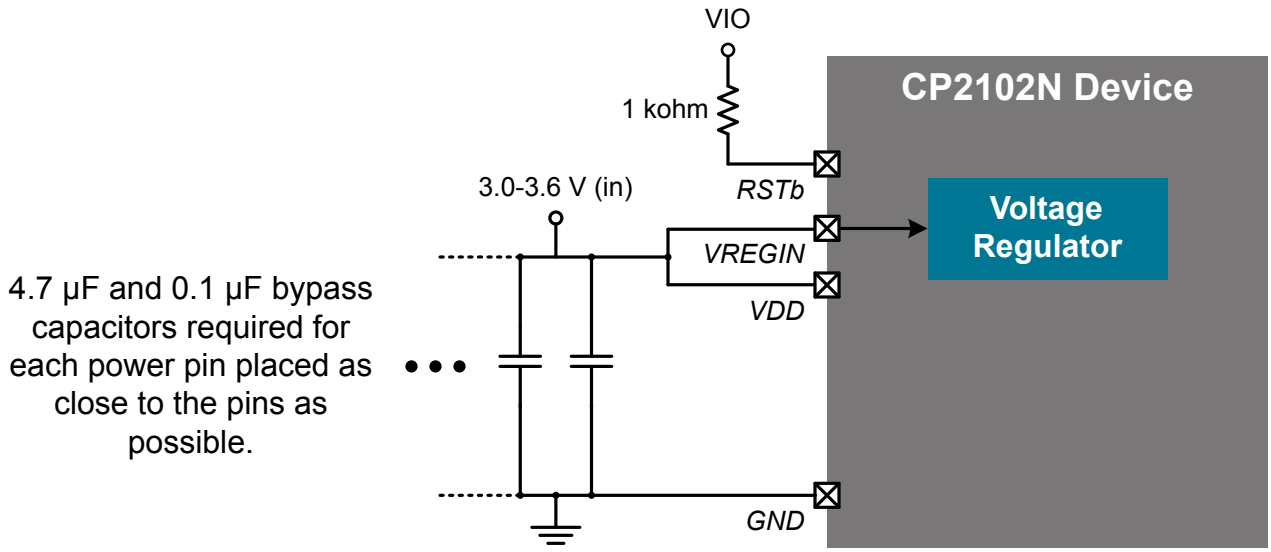


Figure 2.3. Connection Diagram with Voltage Regulator Not Used

2.2 Battery Charger Detect

The CP2102N Battery Charger Detect notifies an external battery charger the amount of current available from the USB interface.

The figure below shows an example connection diagram for external battery charging circuitry. If using an external battery charging IC, consult the data sheet for more information about the specific recommended connection diagrams.

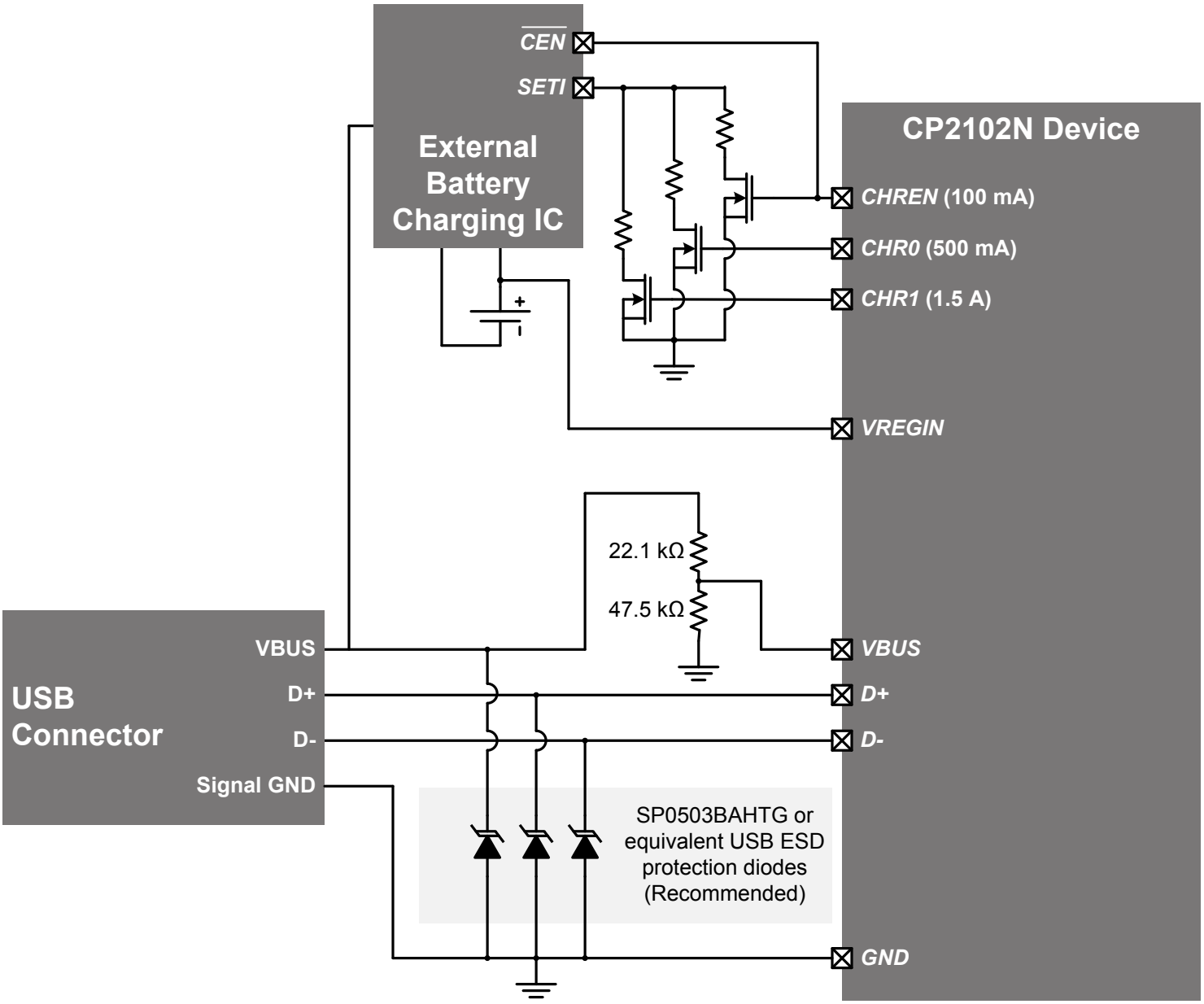


Figure 2.4. Battery Charging Connection Diagram

2.3 USB

The figure below shows a typical connection bus-powered diagram for the USB pins of the CP2102N devices including ESD protection diodes on the USB pins.

Note: There are two relevant restrictions on the VBUS pin voltage in self-powered and bus-powered configurations. The first is the absolute maximum voltage on the VBUS pin, which is defined as VIO + 2.5 V in Table 3.10 Absolute Maximum Ratings on page 15. The second is the Input High Voltage (VIH) for VBUS to detect when the device is connected to a bus, which is defined as VIO – 0.6 V in Table 3.7 GPIO on page 13. A resistor divider (or functionally-equivalent circuit) on VBUS is required to meet these specifications and ensure reliable device operation. In this case, the current limitation of the resistor divider prevents high VBUS pin leakage current, even though the VIO + 2.5 V specification is not strictly met while the device is not powered.

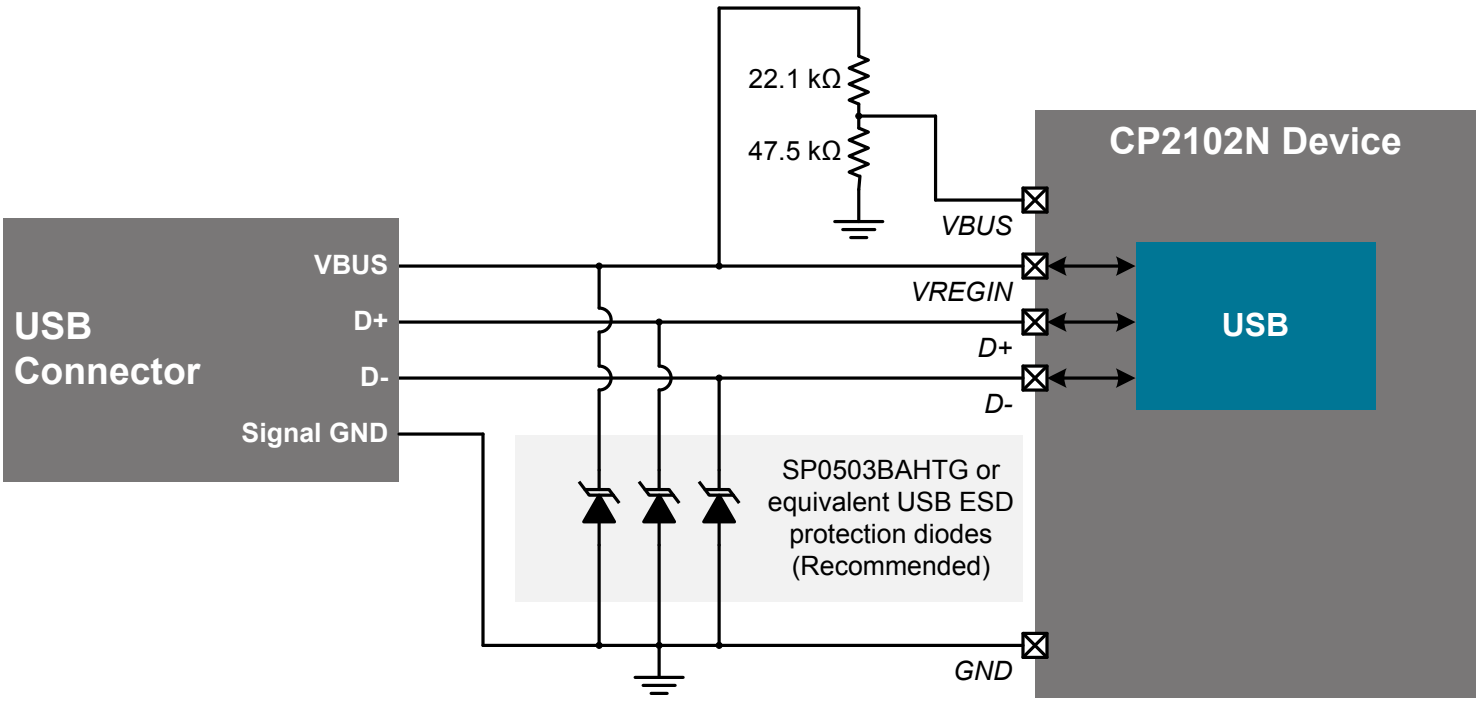


Figure 2.5. Bus-Powered Connection Diagram for USB Pins

The figure below shows a typical connection self-powered diagram for the USB pins of the CP2102N devices including ESD protection diodes on the USB pins.

Note: There are two relevant restrictions on the VBUS pin voltage in self-powered and bus-powered configurations. The first is the absolute maximum voltage on the VBUS pin, which is defined as VIO + 2.5 V in Table 3.10 Absolute Maximum Ratings on page 15. The second is the Input High Voltage (VIH) for VBUS to detect when the device is connected to a bus, which is defined as VIO – 0.6 V in Table 3.7 GPIO on page 13. A resistor divider (or functionally-equivalent circuit) on VBUS is required to meet these specifications and ensure reliable device operation. In this case, the current limitation of the resistor divider prevents high VBUS pin leakage current, even though the VIO + 2.5 V specification is not strictly met while the device is not powered.

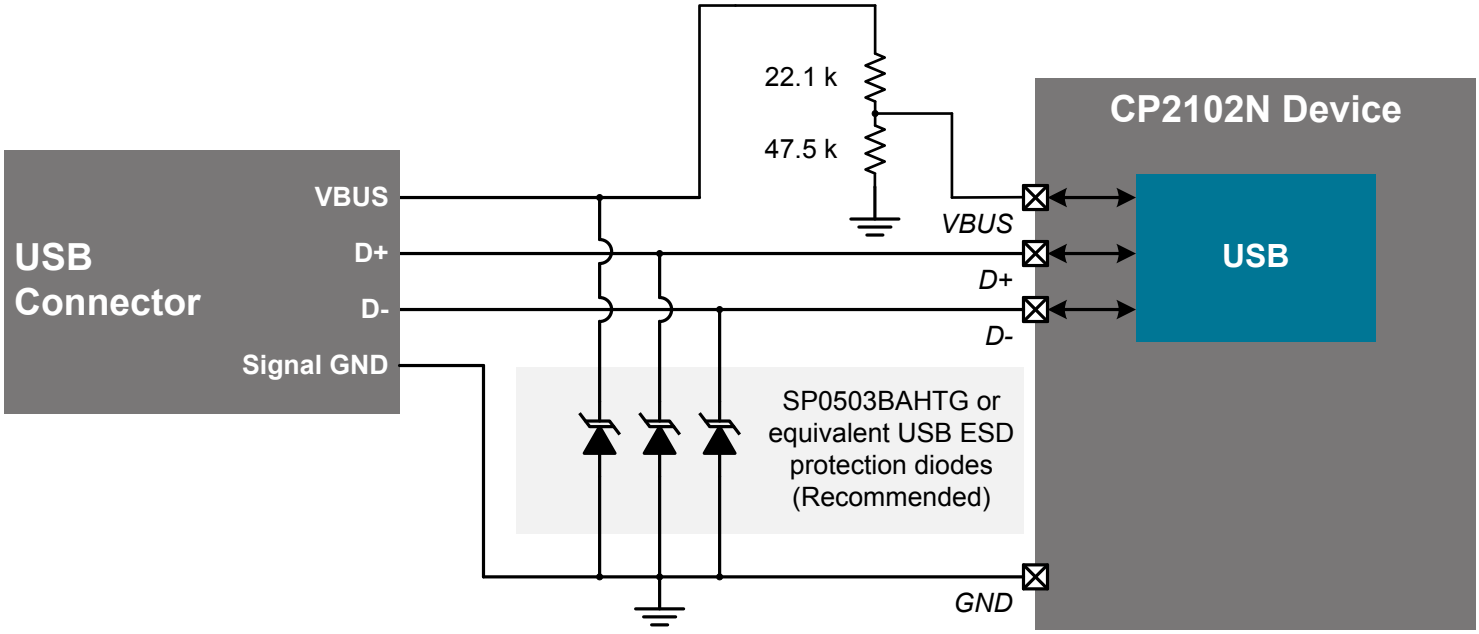


Figure 2.6. Self-Powered Connection Diagram for USB Pins

3. Electrical Specifications

3.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 3.1 Recommended Operating Conditions on page 10, unless stated otherwise.

3.1.1 Recommended Operating Conditions

Table 3.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD [1]	V_{DD}		3.0	—	3.6	V
Operating Supply Voltage on VIO [3]	V_{IO}		1.71	—	V_{DD}	V
Operating Supply Voltage on VREGIN	V_{REGIN}		3.0	—	5.25	V
Operating Ambient Temperature	T_A		-40	—	85	°C

Note:

1. Standard USB compliance tests require 3.0 V on VDD for compliant operation.
2. All voltages with respect to GND.
3. On devices without a VIO pin, $V_{IO} = V_{DD}$.
4. GPIO levels are undefined whenever VIO is less than 1 V.

3.1.2 Power Consumption

Table 3.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Normal Operation[1, 2]	I_{DD}	115200 baud transmitting continuous bidirectional data	—	9.5	—	mA
		3 Mbaud transmitting continuous bidirectional data	—	13.7	—	mA
USB Suspend[1, 2]	I_{DD}		—	195	—	µA
Held in Reset[1, 2]	I_{DD}		—	1.3	—	mA
USB Pull-up[3]	I_{PU}		—	200	230	µA

Note:

1. Includes supply current from internal LDO regulator, supply monitor, and internal oscillators. These power consumption numbers are only for the CP2102N and do not include an external RS232 transceiver or other external circuitry.
2. USB Pull-up current should be added for total supply current. Normal and suspended supply current is current flowing into VREGIN.
3. The USB Pull-up supply current values are calculated values based on USB specifications. USB Pull-up supply current is current flowing from VDD to GND through USB pull-down/pull-up resistors on D+ and D-.

3.1.3 Reset and Supply Monitor

Table 3.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V_{VDDM}		1.95	2.05	2.15	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on VDD	—	1.2	—	V
		Falling Voltage on VDD	0.75	—	1.36	V
VDD Ramp Time	t_{RMP}	Time to V_{DD} > 2.2 V	10	—	—	µs
Reset Delay from POR	t_{POR}	Relative to V_{DD} > V_{POR}	3	10	31	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	50	—	µs
RSTb Low Time to Generate Reset	t_{RSTL}		15	—	—	µs

Note:
1. The RSTb pin will be driven low during power-on and power failure reset events.

3.1.4 Configuration Memory

Table 3.4. Configuration Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
V_{DD} Voltage During Programming [1]	V_{PROG}		3.0	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles

Note:
1. The device can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).
2. Data Retention Information is published in the Quarterly Quality and Reliability Report.

3.1.5 Internal Oscillator

Table 3.5. Internal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Oscillator Frequency	f_{OSC}	Full Temperature and Supply Range	47.3	48	48.7	MHz
Power Supply Sensitivity	PSS_{OSC}	T_A = 25 °C	—	0.02	—	%/V
Temperature Sensitivity	TS_{OSC}	V_{DD} = 3.0 V	—	45	—	ppm/°C

3.1.6 5 V Voltage Regulator

Table 3.6. 5V Voltage Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage Range [1]	V_{REGIN}		3.0	—	5.25	V
Output Voltage on VDD [2]	V_{REGOUT}	Output Current = 1 to 100 mA Regulation range (VREGIN ≥ 4.1V)	3.1	3.3	3.6	V
		Output Current = 1 to 100 mA Dropout range (VREGIN < 4.1V)	—	V_{REGIN} – $V_{DROPOUT}$	—	V
Output Current [2]	I_{REGOUT}		—	—	100	mA
Dropout Voltage	$V_{DROPOUT}$	Output Current = 100 mA	—	—	0.8	V

Note:

1. Input range to meet the Output Voltage on VDD specification. If the 5 V voltage regulator is not used, VREGIN should be tied to VDD.
2. Output current is total regulator output, including any current required by the device.

3.1.7 GPIO

Table 3.7. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)	V_{OH}	I_{OH} = -7 mA, V_{IO} ≥ 3.0 V	V_{IO} - 0.7	—	—	V
		I_{OH} = -3.3 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OH} = -1.8 mA, 1.71 V ≤ V_{IO} < 2.2 V	V_{IO} x 0.8	—	—	V
Output Low Voltage (High Drive)	V_{OL}	I_{OL} = 13.5 mA, V_{IO} ≥ 3.0 V	—	—	0.6	V
		I_{OL} = 7 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OL} = 3.6 mA, 1.71 V ≤ V_{IO} < 2.2 V	—	—	V_{IO} x 0.2	V
Output High Voltage (Low Drive)	V_{OH}	I_{OH} = -4.75 mA, V_{IO} ≥ 3.0 V	V_{IO} - 0.7	—	—	V
		I_{OH} = -2.25 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OH} = -1.2 mA, 1.71 V ≤ V_{IO} < 2.2 V	V_{IO} x 0.8	—	—	V
Output Low Voltage (Low Drive)	V_{OL}	I_{OL} = 6.5 mA, V_{IO} ≥ 3.0 V	—	—	0.6	V
		I_{OL} = 3.5 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OL} = 1.8 mA, 1.71 V ≤ V_{IO} < 2.2 V	—	—	V_{IO} x 0.2	V
Input High Voltage (all GPIO pins including VBUS)	V_{IH}		V_{IO} - 0.6	—	—	V
Input Low Voltage (all GPIO including VBUS)	V_{IL}		—	—	0.6	V
Pin Capacitance	C_{IO}		—	7	—	pF
Weak Pull-Up Current (V_{IN} = 0 V)	I_{PU}	V_{DD} = 3.6	-30	-20	-10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	GND < V_{IN} < V_{IO}	-1.1	—	1.1	µA
Input Leakage Current with V_{IN} above V_{IO}	I_{LK}	V_{IO} < V_{IN} < V_{IO}+2.0 V	0	5	150	µA
RS485 Setup Time before Start Bit[1]	t_{RS485S}		0	—	64.02	ms
RS485 Hold Time after Stop Bit[1]	t_{RS485H}		0	—	64.02	ms
TX Toggle Rate	$f_{TXTOGGLE}$		—	20	—	Hz
RX Toggle Rate	$f_{RXTOGGLE}$		—	20	—	Hz

Note:

1. Programmable from 0 ms to 64 ms in 1 µs steps. The programmed time is the guaranteed minimum, and the actual time may be up to 20 µs longer.

3.1.8 USB Transceiver

Table 3.8. USB Transceiver

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmitter						
Output High Voltage	V_{OH}	$V_{DD} \geq 3.0V$	2.8	—	—	V
Output Low Voltage	V_{OL}	$V_{DD} \geq 3.0V$	—	—	0.8	V
Output Crossover Point	V_{CRS}		1.3	—	2.0	V
Output Impedance	Z_{DRV}	Driving High	28	36	44	Ω
		Driving Low	28	36	44	
Pull-up Resistance	R_{PU}	Full Speed (D+ Pull-up)	1.425	1.5	1.575	kΩ
Output Rise Time	T_R	Full Speed	4	—	20	ns
Output Fall Time	T_F	Full Speed	4	—	20	ns
Receiver						
Differential Input Sensitivity	V_{DI}	| (D+) - (D-) |	0.2	—	—	V
Differential Input Common Mode Range	V_{CM}		0.8	—	2.5	V
Input Leakage Current	I_L	Pullups Disabled	—	<1.0	—	µA
Refer to the USB Specification for timing diagrams and symbol definitions.						

3.2 Thermal Conditions

Table 3.9. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient)	θ_{JA}	QFN20 Packages	—	60	—	°C/W
		QFN24 Packages	—	30	—	°C/W
		QFN28 Packages	—	26	—	°C/W
Thermal Resistance (Junction to Case)	θ_{JC}	QFN20 Packages	—	32.9	—	°C/W
		QFN24 Packages	—	24.2	—	°C/W
		QFN28 Packages	—	18.8	—	°C/W
Thermal Characterization Parameter (Junction to Top)	Ψ_{JT}	QFN20 Packages	—	0.88	—	°C/W
		QFN24 Packages	—	0.3	—	°C/W
		QFN28 Packages	—	0.3	—	°C/W

Note:
1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

3.3 Absolute Maximum Ratings

Stresses above those listed in 3.3 Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 3.10. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		-55	125	°C
Storage Temperature	T_{STG}		-65	150	°C
Voltage on VDD	V_{DD}		GND-0.3	4.2	V
Voltage on VIO[2]	V_{IO}		GND-0.3	4.2	V
Voltage on VREGIN	V_{REGIN}		GND-0.3	5.8	V
Voltage on D+ or D-	V_{USBD}		GND-0.3	V_{DD}+0.3	V
Voltage on UART pins, GPIO, VBUS, RSTb, or any other non-power, non-USB pin	V_{IN}	V_{IO} > 3.3 V	GND-0.3	5.8	V
		V_{IO} < 3.3 V	GND-0.3	V_{IO}+2.5	V
Total Current Sunk into Supply Pin	I_{VDD}		—	400	mA
Total Current Sourced out of Ground Pin	I_{GND}		400	—	mA
Current Sourced or Sunk by any UART pins, GPIO, VBUS, RSTb, or any other non-power, non-USB pin	I_{IO}		-100	100	mA
Operating Junction Temperature	T_J		-40	105	°C

Note:

1. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. On devices without a VIO pin, $V_{IO} = V_{DD}$

3.4 Typical Performance Curves

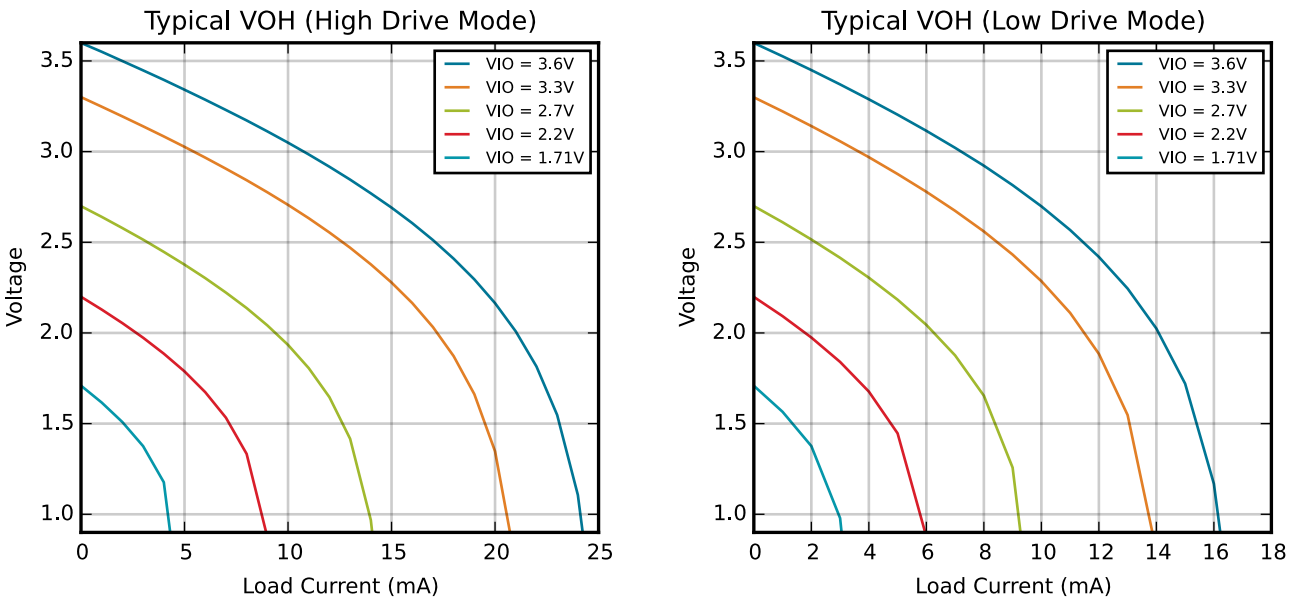


Figure 3.1. Typical V_{OH} Curves

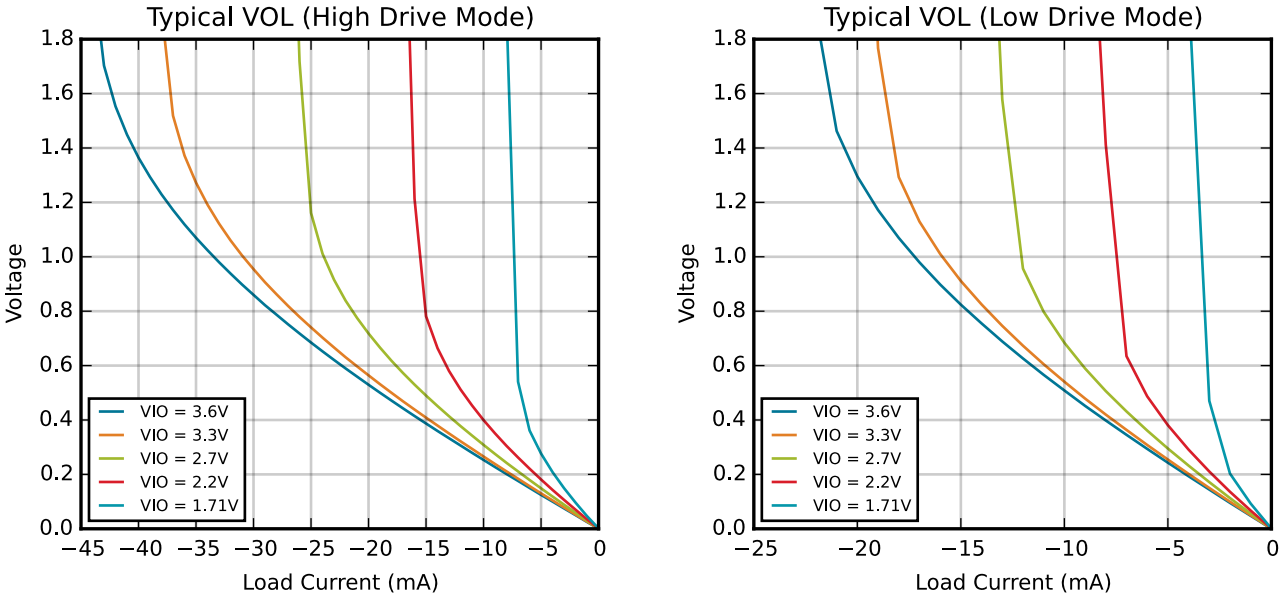


Figure 3.2. Typical V_{OL} Curves

4. Functional Description

4.1 USB Function Controller and Transceiver

The Universal Serial Bus function controller in the CP2102N is a USB 2.0 compliant full-speed device with integrated transceiver and on-chip matching and pull-up resistors. The USB function controller manages all data transfers between the USB and the UART as well as command requests generated by the USB host controller and commands for controlling the function of the UART.

The USB Suspend and Resume signals are supported for power management of both the CP2102N device as well as external circuitry. The CP2102N will enter Suspend mode when Suspend signaling is detected on the bus. On entering Suspend mode, the CP2102N asserts the SUSPEND and SUSPENDb signals. SUSPEND and SUSPENDb are also asserted after a CP2102N reset until device configuration during USB Enumeration is complete.

The CP2102N exits Suspend mode when any of the following occur:

1. Resume signaling is detected or generated.
2. A USB Reset signal is detected.
3. A device reset occurs.
4. USB Remote Wakeup functionality is enabled and the WAKEUP pin is grounded.

On exit of Suspend mode, the SUSPEND and SUSPENDb signals are de-asserted. Both SUSPEND and SUSPENDb temporarily float high during a CP2102N reset. If this behavior is undesirable, a strong pull-down (10 kΩ) can be used to ensure SUSPENDb remains low during reset.

4.2 Universal Asynchronous Receiver/Transmitter (UART) Interface

The CP2102N UART interface consists of the TX (transmit) and RX (receive) data signals as well as the RTS, CTS, DSR, DTR, DCD, and RI control signals. The UART supports RTS/CTS, DSR/DTR, and Xon/Xoff handshaking.

The UART is programmable to support a variety of data formats and baud rates. If the Virtual COM Port drivers are used, the data format and baud rate are set during COM port configuration on the PC. If the USBXpress drivers are used, the CP2102N is configured through the USBXpress API. The data formats and baud rates available are listed in the table below.

Table 4.1. Data Formats and Baud Rates

Parameter	Available Values
Data Bits	5, 6, 7, and 8
Stop Bits	1, 1.5[1], and 2
Party Types	none, even, odd, mark, space
Baud Rates	300, 600, 1200, 1800, 2400, 4000, 4800, 7200, 9600, 14400, 16000, 19200, 28800, 38400, 51200, 56000, 57600, 64000, 76800, 115200, 128000, 153600, 230400, 250000, 256000, 460800, 500000, 576000, 921600, 1000000, 1200000, 1500000, 2000000, 3000000

Note:
1. 5-bit only.

4.2.1 Baud Rate Generation

The baud rate generator is very flexible, allowing the user to request any baud rate in the range from 300 baud to 3 Mbaud. If the baud rate cannot be directly generated from the 48 MHz oscillator, the device will choose the closest possible option. The actual baud rate is dictated by the following equations.

$$\text{Clock Divider} = \frac{48\ \text{MHz}}{2 \times \text{Prescale} \times \text{Requested Baud Rate}}$$

$$\text{Actual Baud Rate} = \frac{48\ \text{MHz}}{2 \times \text{Prescale} \times \text{Clock Divider}}$$

In both cases, the Prescale value is 4 if the Requested Baud Rate is ≤ 365 baud and 1 if the Requested Baud Rate value is > 365 baud.

Most baud rates can be generated with an error of less than 1.0%. A general rule of thumb for the majority of UART applications is to limit the baud rate error on both the transmitter and the receiver to no more than ±2%. The Clock Divider value is rounded to the nearest integer, which may produce an error source. Another error source will be the 48 MHz oscillator, which is accurate to ±0.25%. Knowing the actual and requested baud rates, the total baud rate error can be found using the equation below.

$$\text{Baud Rate Error (\%)} = 100 \times \left(1 - \frac{\text{Actual Baud Rate}}{\text{Requested Baud Rate}}\right) \pm 0.25\%$$

4.2.2 Sending Break Signaling

The CP2102N supports break signaling with an external 10k Ohm resistor between TXD and ground. This resistor is sufficient for break signaling across all baud rates.

When a Send Break command is received, the CP2102N halts adding new data to the transmitter FIFO and will wait 6 byte times for in-flight data to complete transmission. It will not process other USB transactions such as RX data reception or GPIO commands while waiting - transactions will be processed once break is initiated. During this time, if enabled, the RS-485 signal will begin asserting. If RTS TX Control is enabled, RTS will also begin asserting. Once the 6 byte time has expired, the CP2102N places the TXD line in a high-impedance state - ignoring flow control status - and the external resistor pulls down TXD to initiate a break.

While sending break the TXT LED toggle is active. USB transactions including RX data reception and GPIO commands function normally.

When a Stop Break command is received, the CP2102N removes TXD from the high impedance state. It is held for 1 byte time to allow for stabilization. After that time has expired the transmitter resumes normal operations, and the RS485 and RTS (if RTS TX Control is enabled) signals wait the specified hold time.

4.3 Additional Features

4.3.1 General Purpose Input/Outputs (GPIO)

The CP2102N has up to 7 GPIO that can be controlled from the host. By default and during reset, these pins are set to open-drain with a weak pull-up enabled and the port latch set to 1. The pins can be made push-pull to drive external circuitry like LEDs. In addition, the state of these pins can be configured during standard operation, during Suspend, and immediately following reset.

Note: All pins temporarily float high during a device reset. If this behavior is undesirable, a strong pull-down (10 kΩ) can be used to ensure the pin remains low during reset.

The GPIO pins may also have alternate functions which are listed in the table below.

Table 4.2. GPIO Pin Alternate Functions

GPIO Pin	QFN28 Package	QFN24 Package	QFN20 Package
GPIO.0	TXT	TXT	CLK[1]
GPIO.1	RXT	RXT	RS485
GPIO.2	RS485	RS485	TXT
GPIO.3	WAKEUP	WAKEUP	RXT
GPIO.4	No alternate function	Not available	Not available
GPIO.5	No alternate function	Not available	Not available
GPIO.6	No alternate function	Not available	Not available

Note:
1. On QFN28 and QFN24 packages, the CLK signal is available on the same pin as RI.

By default, all of the GPIO pins are configured as a GPIO input. The speed of reading and writing the GPIO pins is subject to the timing of the USB bus. GPIO pins configured as inputs or outputs are not recommended for real-time signaling.

More information regarding the configuration of these pins can be found in Xpress Configurator in Simplicity Studio and *AN721: CP21xx Device Customization Guide*. Guidance on GPIO usage can be found in *AN223: Runtime GPIO Control for CP210x*.

4.3.2 Dynamic Suspend

By default, the latch values for all pins remains static during USB Suspend.

Alternatively, the dynamic suspend feature sets the pin latch to a predefined state when the CP2102N device moves from the configured USB state to the suspend USB state (see chapter nine of USB 2.0 specification for more information on USB device states). When the device exits the suspend USB state, the pin latch is restored to the previous value before entering the suspend state. Dynamic Suspend is configured separately for the GPIO pins and UART/Modem Control pins.

4.3.3 Output Mode

Each pin has two options for the output mode: push-pull and open-drain.

By configuring for push-pull operation, a pin operates as a push-pull output. The output voltage is determined by pin's latch value. This type of output is most often used to connect directly to another device or drive external circuitry like an LED.

By configuring for open-drain operation, a pin operates as an open-drain output or input. The output voltage is determined by the pin's latch value. If the pin latch value is 1, the pin is pulled up to VIO (or VDD if the device does not have a VIO pin) through an on-chip pull-up resistor. Open-drain outputs are typically used when interfacing to logic at a higher voltage than the VIO pin. These pins can be safely pulled to the higher, external voltage through an external pull-up resistor if VDD meets the 3.3 Absolute Maximum Ratings requirements.

4.3.4 Battery Charging (CHREN, CHR0, and CHR1)

When battery charging is enabled, the D+/D- signals will detect the type of current source attached and set the CHREN, CHR0, and CHR1 pins appropriately. CHREN enables 100 mA source current, CHR0 enables 500 mA source current, and CHR1 enables 1.5 A source current.

The charging system may draw up to the limit specified by CHREN, CHR0, and CHR1. If the system also is operational while charging, the current set points for the ISET resistors should be decreased based on how much the system could be using during battery charge.

When configuring a device to enable battery charging, the GPIO associated with the battery charging pins must also be configured correctly in Xpress Configurator as shown in the following table.

Table 4.3. Configuring GPIO for Battery Charging

Charge Detect Mode	Pins	State
Up to 100 mA	CHREN	Push-Pull/High
	CHR1	Open Drain/Low
	CHR0	Open Drain/Low
Up to 500 mA	CHREN	Push-Pull/High
	CHR1	Open Drain/Low
	CHR0	Push-Pull/High
Above 500 mA	CHREN	Push-Pull/High
	CHR1	Push-Pull/High
	CHR0	Push-Pull/High

Note: Battery charging pins (CHREN, CHR1, CHR0) are disabled in Suspend only when using a Standard Data Port. If attached to a Dedicated Charging Port or Charging Downstream Port, the battery charging pins are left on while in Suspend.

4.3.5 Remote Wakeup (WAKEUP)

The WAKEUP pin is an optional active low remote wakeup input. When the wakeup pin toggles from inactive to active (i.e. grounded) and the CP2102N is in USB suspend, the CP2102N will begin the wakeup sequence.

Host software must enable USB remote wakeup for the device. In Windows, this is under Device Manager. To set this, right-click on the device, select [**Properties**]>[**Power Management**] and enable the [**Allow this device to wake the computer**] feature.

4.3.6 Clock Output (CLK)

An optional clock output is available on CP2102N devices.

$$F_{CLK} = \frac{48\ \text{MHz}}{2 \times N}$$

The valid values for N are 1 to 256.

Note: The clock output stops and is no longer present on the pin when the CP2102N device is in USB Suspend. This occurs when the device is connected to USB and the host controller suspends the device (either through a feature like Selective Suspend or when the host PC is in Hibernate or Sleep modes) or when the CP2102N is disconnected from the host in self-powered mode.

4.3.7 Hardware Handshaking (RTS and CTS)

To utilize the functionality of the RTS and CTS pins of the CP2102N, the device must be configured to use hardware flow control on the USB host.

RTS, or Ready To Send, is an active-low output from the CP2102N and indicates to the external UART device that the CP2102N's UART RX FIFO has not reached the FLOW OFF watermark level of 448 bytes and is ready to accept more data. When the amount of data in the RX FIFO reaches the watermark, the CP2102N pulls RTS high to indicate to the external UART device to stop sending data. The CP2102N does not pull RTS low again until the UART RX FIFO is at the FLOW ON watermark level of 384 bytes (at least 128 free bytes). This hysteresis allows for optimal operation. These RTS watermark levels are configurable using Xpress Configurator in Simplicity Studio.

Note: RTS TX Control signaling is a special mode that asserts RTS while the CP2102N is transmitting. This mode is not available below 300 baud. RTS hardware flow control works at all baud rates.

CTS, or Clear To Send, is an active-low input to the CP2102N and is used by the external UART device to indicate to the CP2102N when the external UART device's RX FIFO is getting full. The CP2102N will not send more than two bytes of data once CTS is pulled high.

Hardware handshaking allows for optimal continuous transmission speeds at high baud rates (greater than 1 MBaud). The effective throughput depends on USB bus loading and host USB stack efficiency. The typical maximum continuous bidirectional data transfer is > 450 kbytes/s at 3 Mbaud.

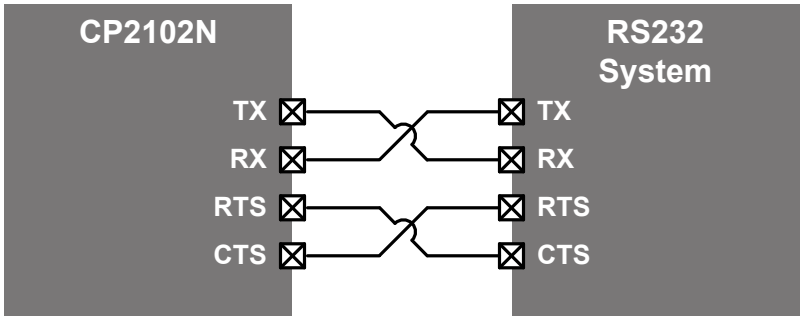


Figure 4.1. Using Hardware Flow Control with the CP2102N

4.3.8 Software Handshaking

The CP2102N also supports software handshaking using the XON and XOFF event characters. The characters used for XON/XOFF is set by the host software.

If the CP2102N receives an XOFF request, it will stop transmission, even if the CP2102N receiver needs to transmit an XOFF over UART. This can potentially allow an overflow to occur or a deadlock condition if both the CP2102N and the connected UART device transmit XOFF at the same time. The XOFF_CONTINUE setting allows the CP2102N transmitter to send XOFF/XON requests even if it has received an XOFF request from the connected UART device. Once the connected UART device transmits XON, normal transmission from the CP2102N resumes.

Software handshaking uses the same watermark levels as hardware handshaking and can be configured dynamically by host software. Watermark levels greater than 512 are converted to an XON limit of 192 bytes and an XOFF limit of 64 bytes. If the XON limit crosses over the XOFF limit, the XON limit will automatically be modified to not cross over the XOFF limit. An XOFF limit of 0 is converted to 64 to guarantee buffer space is available until the UART end device stops transmission. When setting the XON and XOFF limits, it's recommended to use values where the XON limit added to the XOFF limit is less than 512 bytes, like 192/192 or 128/128. CP2102N testing shows that the XON limit set to 192 and XOFF limit set to 192 provides optimal software flow control behavior.

Figure 4.2. Software Flow Control Timing Diagram

4.3.9 Data Throughput Optimization

Effective throughput depends on several factors:

- CP2102N placement on the physical USB device tree
- USB bus load from other devices
- Host OS USB stack efficiency
- CP2102N configuration options

Handshaking is required at high baud rates (greater than 1 MBaud) to avoid receiver overrun. A request to stop transmission is only initiated once the RX FIFO has reached the FLOW OFF watermark level. Once the USB bus lowers the RX FIFO level below the FLOW ON watermark, a request to continue transmission is sent.

Hardware handshaking allows for optimal continuous transmission speeds at high baud rates. Using a Windows host PC, the CP2102N's typical maximum continuous bidirectional throughput is > 450 kbytes/s at 3 Mbaud (> 70% efficiency).

Software handshaking using XON/XOFF transmission requires more overhead. Using a Windows host PC, the CP2102N's typical maximum continuous bidirectional throughput is > 330 kbytes/s at 3 Mbaud (> 55% efficiency).

For these performance numbers, the CP2102N is placed on a USB hub connected to the Windows host PC with a third party UART adapter. The only significant USB traffic is generated by the USB to UART devices. The Windows host PC is running automated tests with minimal CPU load.

Certain conditions will reduce the maximum throughput at high baud rates (> 1Mbaud):

- Using DSR, DTR, or DCD handshaking signals lowers maximum performance. Use hardware CTS/RTS only for peak performance.
- Embedded events or error character insertion requires free space in the UART RX FIFO to post events to the host. At high baud rates with continuous data reception, this space may not be available. Limit maximum baud rates with continuous data reception to 1 MBaud when using embedded events or error character insertion to guarantee reception of events or the error character.
- Transmitting an immediate character momentarily causes lower bidirectional throughput as the character forces a bypass of the current transmit FIFO. Once the character has been transmitted, the typical bidirectional throughput is restored.

Using Remote Wakeup, Charge Enable, Clock Out, or the GPIOs will not impact UART throughput.

4.3.10 Transmit and Receive LED Toggles (TXT and RXT)

The TX and RX LED toggle pins will toggle on and off at a fixed rate specified in Table 3.7 GPIO on page 13 whenever a byte is transmitted or received by the CP2102N. These pins are logic high whenever a device is not transmitting or receiving data and can directly drive basic LEDs within the device specification limits.

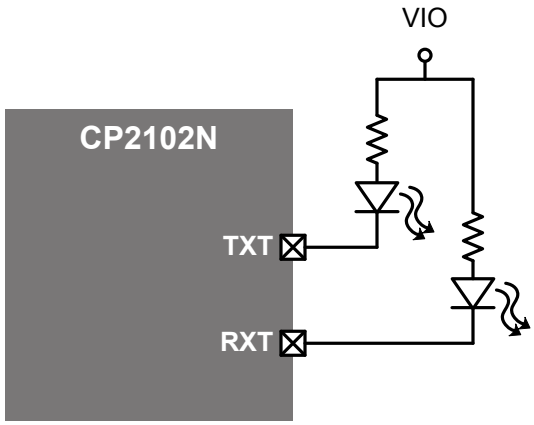


Figure 4.3. Transmit and Receive Toggle

4.3.11 Modem Control (DSR, DTR, DCD, RI)

The modem control pins are enabled when requested on the host. If the Virtual COM Port drivers are used, the modem control pins are enabled during COM port configuration on the PC. If the USBXpress drivers are used, the CP2102N is configured through the USBXpress API. The behavior of the modem control pins may vary between operating systems.

Table 4.4. Modem Control Signals

Modem Control Signal	Description
DSR	Input to the CP2102N. Data Set Ready control input (active low).
DTR	Output from the CP2102N. Data Terminal Ready control output (active low). Note that this pin may toggle when opening a COM port on some operating systems.
DCD	Input to the CP2102N. Data Carrier Detect control input (active low).
RI	Input to the CP2102N. Ring Indicator control input (active low).

4.3.12 RS485 (RS485)

The RS485 pin is an optional control pin that can be connected to the DE and RE inputs of the transceiver. When configured for RS485 mode, the pin is asserted during UART data transmission. The RS485 pin is active-high by default and is also configurable for active-low mode using Xpress Configurator.

The RS485 pin setup and hold times are programmable using Xpress Configurator to enable maximum flexibility.

Note: Note The RS485 pin is not available at baud rates below 300 baud.

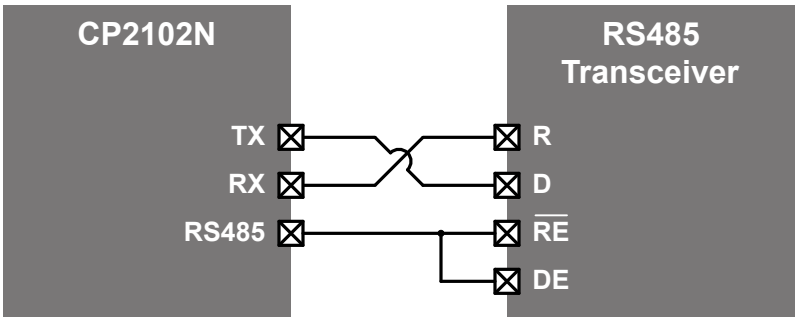


Figure 4.4. Using the CP2102N with a RS485 Transceiver

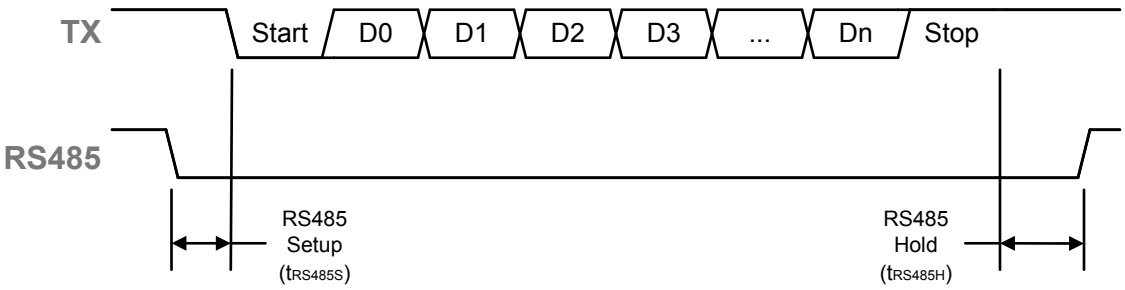


Figure 4.5. RS485 Output Timing Diagram for a Single-Byte Transfer

4.3.13 Receiver Timeout

The CP2102N supports a new custom vendor command to configure the internal buffer receive timeout. During normal operation, when data is received the receive buffer waits up to 2 ms or 128 character times, whichever is fewer, before transferring data to host. This timer is reset each time new data is received. For some usage models, this response time causes unwanted extra latency between receiving a byte at the UART and the byte being available on the host. The Set Receiver Max Timeout custom vendor command allows applications to set the timeout from .001 ms to 2 ms. Small values will cause the receiver to inefficiently use the 512 byte Receive Buffer and should not be used at high data rates (greater than 230400).

4.4 Drivers

There are two sets of device drivers available for the CP2102N devices: the Virtual COM Port (VCP) drivers and the USBXpress Direct Access drivers. Only one set of drivers is necessary to interface with the device.

The latest drivers are available at www.silabs.com/interface-software.

4.4.1 Virtual COM Port (VCP) Drivers

The CP2102N Virtual COM Port (VCP) device drivers allow a CP2102N-based USB device to appear to the PC's application software as a COM port. Application software running on the PC accesses the CP2102N-based device as it would access a standard hardware COM port. However, actual data transfer between the PC and the CP2102N device is performed over the USB interface. Therefore, existing COM port applications may be used to transfer data via the USB to the CP2102N-based device without modifying the application. See *AN197: Serial Communications Guide for the CP210x* for Example Code for Interfacing to a CP2102N using the Virtual COM drivers.

Note: Because the CP2102N uses a USB-based communication interface, timing will not be controllable or guaranteed as it is with a standard COM port. Full-speed USB operates on 1 ms frames, and the host schedules packets for each USB device where it can in the 1 ms frame. It is recommended to use large data transfers when reading and writing from the host to send data as quickly as possible.

4.4.2 USBXpress Drivers

The Silicon Labs USBXpress drivers provide an alternate solution for interfacing with CP2102N devices. No serial port protocol expertise is required. Instead, a simple, high-level application program interface (API) is used to provide simpler CP210x connectivity and functionality. The USBXpress for CP210x Development Kit includes Windows device drivers, Windows device driver installer and uninstallers, and a host interface function library (host API) provided in the form of a Windows Dynamic Link Library (DLL). The USBXpress driver set is recommended for new products that also include new PC software. The USBXpress interface is described in *AN169: USBXpress® Programmer's Guide*.

4.4.3 Customization and Certification

In addition to customizing the device as described in 4.5 Device Customization, the drivers can be also be customized. See *AN220: USB Driver Customization* for more information on generating customized VCP and USBXpress drivers.

The default drivers that are shipped with the CP2102N are Microsoft WHQL (Windows Hardware Quality Labs) certified. The certification means that the drivers have been tested by Microsoft and their latest operating systems will allow the drivers to be installed without any warnings or errors. Some installations of Windows will prevent unsigned drivers from being installed at all. The customized drivers that are generated using the *AN220* software are not automatically certified. They must first go through the Microsoft Driver Reseller Submission process. See *AN807: Recertifying a Customized Windows HCK Driver Package* for more information and contact Silicon Labs support for assistance with this process.

4.5 Device Customization

The CP2102N includes an internal electrically erasable programmable read-only memory (EEPROM). This memory may be used to customize the USB Vendor ID (VID), Product ID (PID), Product Description String, Power Descriptor, Device Release Number and Device Serial Number as desired for OEM applications. If the EEPROM is not programmed with OEM data, the default configuration data shown in the table below is used.

Table 4.5. Default USB Configuration Data

Name	Description	Default Value
Vendor ID (VID)	The Vendor ID is a four digit hexadecimal number that is unique to a particular vendor. 0x10C4, for example, is the Silicon Labs Vendor ID.	0x10C4
Product ID (PID)	The Product ID is a four digit hexadecimal number that identifies the vendor's device. 0xEA60, for example, is the default Product ID for Silicon Labs' CP210x USB to UART Bridge devices.	0xEA60
Power Mode	This setting determines whether the device is Bus-Powered, i.e. it is powered by the host, or Self-Powered, i.e. it is powered from a supply on the device.	0x80 (Bus-Powered)
Max Power	This describes the maximum amount of power that the device will draw from the host in mA multiplied by 2. For example, 0x32 equates to 100 mA.	0x32
Release Version	The Release Version is a binary-coded-decimal value that is assigned by the device manufacturer.	0x0100
Serial String	The Serial String is an optional string that is used by the host to distinguish between multiple devices with the same VID and PID combination. It is limited to 63 characters.	128-bit unique ID assigned by Silicon Labs
Product String	The Product String is an optional string that describes the product. It is limited to 126 characters.	"CP2102N USB to UART Bridge Controller"

While customization of the USB configuration data is optional, it is recommended to customize the VID/PID combination. A unique VID/PID combination will prevent the driver from conflicting with any other USB driver. A vendor ID can be obtained from http://www.usb.org/ or Silicon Labs can provide a free PID for the OEM product that can be used with the Silicon Laboratories VID (http://www.silabs.com/products/mcu/Pages/request-PID.aspx).

If the OEM application supports multiple CP2102N-based devices attached to the same PC, each CP2102N must have a unique serial number. By default, the CP2102N uses a unique 128 bit identifier as the serial number. Alternatively, sequential serial numbers can be pre-programmed by Silicon Labs using settings provided by Xpress Configurator and delivered as a custom CP2102N part number. These serial numbers can be unique per custom part number, or multiple part numbers can share the same group of sequential serial numbers. For more details, see Xpress Configurator in Simplicity Studio.

The internal programmable ROM is programmed via the USB. This allows the OEM's USB configuration data and serial number to be written to the CP2102N on-board ROM during the manufacturing and testing process. A simple GUI-based or command-line customization utility for programming the internal programmable ROM is available from Silicon Labs as a part of Simplicity Studio or available separately on the Silicon Labs website (www.silabs.com/interface-software).

The device parameters can be locked to prevent future modification on the CP2102N.

5. Pin Definitions

5.1 CP2102N QFN28 Pin Definitions

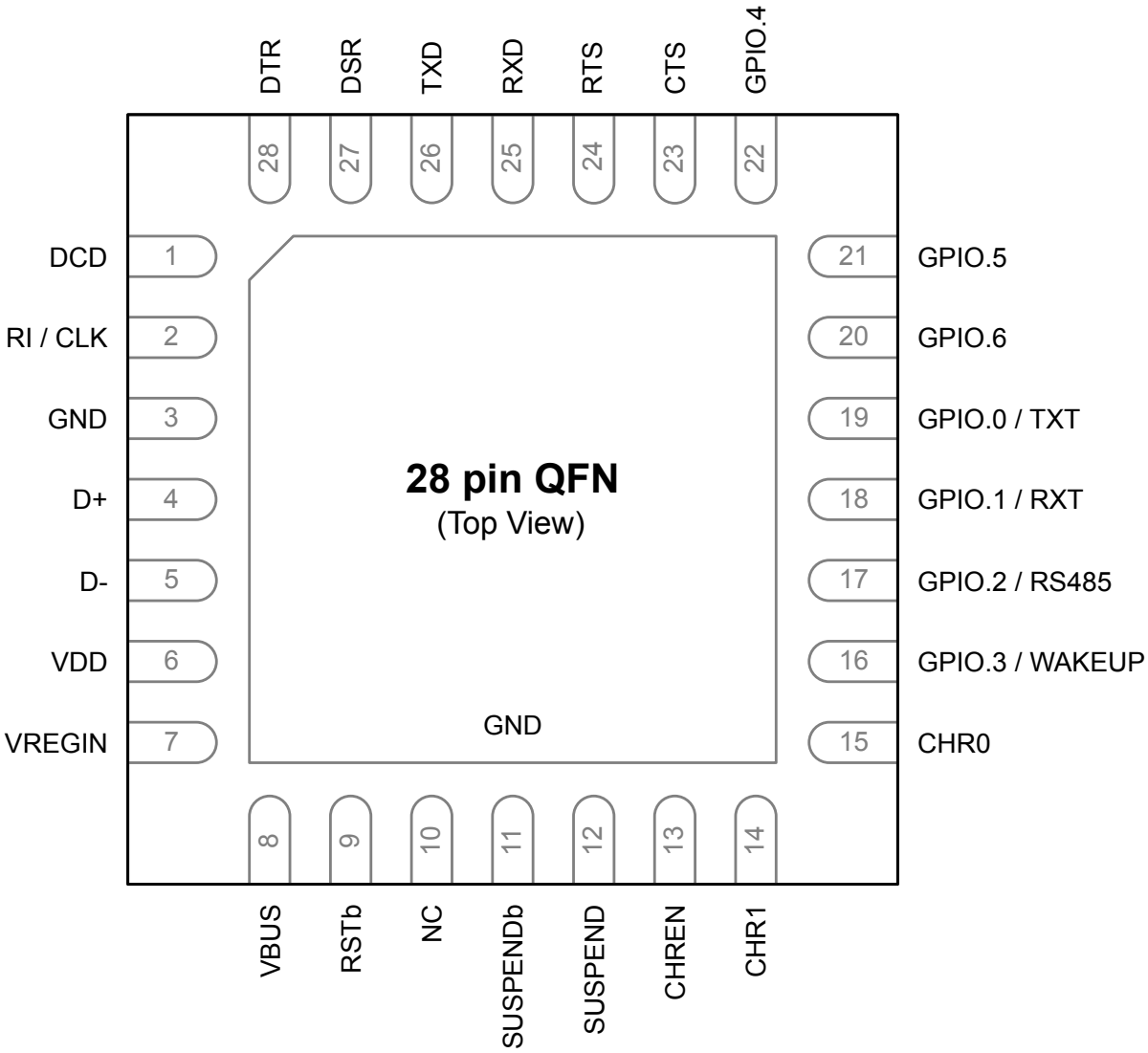


Figure 5.1. CP2102N QFN28 Pinout

Table 5.1. Pin Definitions for CP2102N QFN28

Pin Number	Pin Name	Description
1	DCD	Digital Input. Data Carrier Detect control input (active low).
2	RI / CLK	Digital Input. Ring Indicator control input (active low). Digital Output. Clock output.
3	GND	Ground

Pin Number	Pin Name	Description
4	D+	USB Data Positive
5	D-	USB Data Negative
6	VDD	Supply Power Input / 5V Regulator Output
7	VREGIN	5V Regulator Input
8	VBUS	Digital Input. VBUS Sense Input. This pin should be connected to the VBUS signal of a USB network. A 5 V signal on this pin indicates a USB network connection.
9	RSTb	Active-low Reset
10	NC	No Connect (leave this pin floating).
11	SUSPENDb	Digital Output. This pin is driven low when the device enters the USB suspend state.
12	SUSPEND	Digital Output. This pin is driven high when the device enters the USB suspend state.
13	CHREN	Digital Output. Enable charging circuit (100 mA).
14	CHR1	Digital Output. Enable highest current (1.5 A).
15	CHR0	Digital Output. Enable higher current (500 mA).
16	GPIO.3 / WAKEUP	Digital Input/Output. General Purpose I/O. Digital Input. Remote USB wakeup interrupt input.
17	GPIO.2 / RS485	Digital Input/Output. General Purpose I/O. Digital Output. RS485 control signal.
18	GPIO.1 / RXT	Digital Input/Output. General Purpose I/O. Digital Output. Receive LED toggle.
19	GPIO.0 / TXT	Digital Input/Output. General Purpose I/O. Digital Output. Transmit LED toggle.
20	GPIO.6	Digital Input/Output. General Purpose I/O.
21	GPIO.5	Digital Input/Output. General Purpose I/O.
22	GPIO.4	Digital Input/Output. General Purpose I/O.
23	CTS	Digital Input. Clear To Send control input (active low).
24	RTS	Digital Output. Ready To Send control output (active low).
25	RXD	Digital Input. Asynchronous data input (UART Receive).
26	TXD	Digital Output. Asynchronous data output (UART Transmit).
27	DSR	Digital Input. Data Set Ready control input (active low).
28	DTR	Digital Output. Data Terminal Ready control output (active low).
Center	GND	Ground

5.2 CP2102N QFN24 Pin Definitions

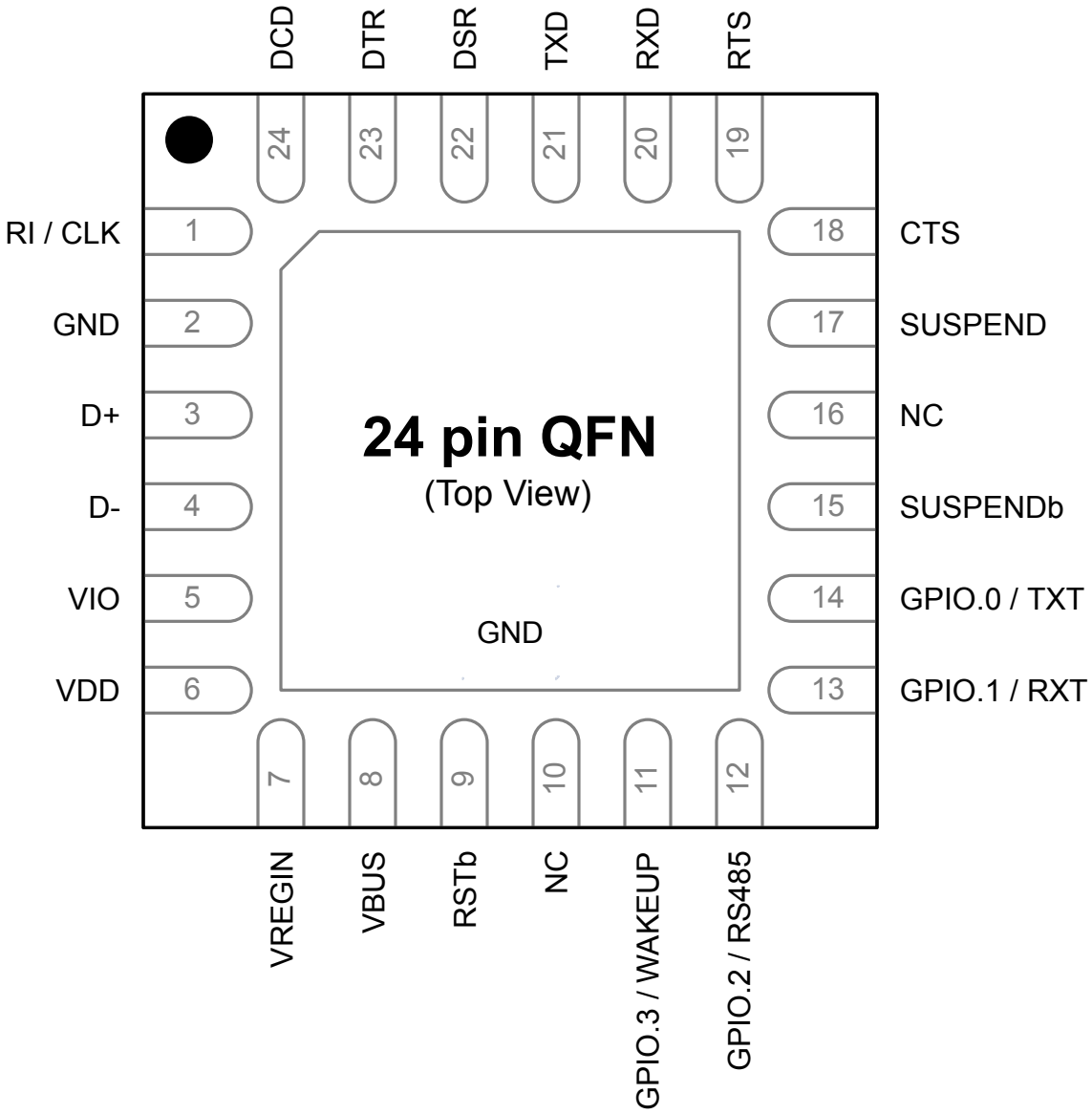


Figure 5.2. CP2102N QFN24 Pinout

Table 5.2. Pin Definitions for CP2102N QFN24

Pin Number	Pin Name	Description
1	RI / CLK	Digital Input. Ring Indicator control input (active low). Digital Output. Clock output.
2	GND	Ground
3	D+	USB Data Positive

Pin Number	Pin Name	Description
4	D-	USB Data Negative
5	VIO	I/O Supply Power Input
6	VDD	Supply Power Input / 5V Regulator Output
7	VREGIN	5V Regulator Input
8	VBUS	Digital Input. VBUS Sense Input. This pin should be connected to the VBUS signal of a USB network. A 5 V signal on this pin indicates a USB network connection.
9	RSTb	Active-low Reset
10	NC	No Connect (leave this pin floating).
11	GPIO.3 / WAKEUP	Digital Input/Output. General Purpose I/O. Digital Input. Remote USB wakeup interrupt input.
12	GPIO.2 / RS485	Digital Input/Output. General Purpose I/O. Digital Output. RS485 control signal.
13	GPIO.1 / RXT	Digital Input/Output. General Purpose I/O. Digital Output. Receive LED toggle.
14	GPIO.0 / TXT	Digital Input/Output. General Purpose I/O. Digital Output. Transmit LED toggle.
15	SUSPENDb	Digital Output. This pin is driven low when the device enters the USB suspend state.
16	NC	No Connect (leave this pin floating).
17	SUSPEND	Digital Output. This pin is driven high when the device enters the USB suspend state.
18	CTS	Digital Input. Clear To Send control input (active low).
19	RTS	Digital Output. Ready To Send control output (active low).
20	RXD	Digital Input. Asynchronous data input (UART Receive).
21	TXD	Digital Output. Asynchronous data output (UART Transmit).
22	DSR	Digital Input. Data Set Ready control input (active low).
23	DTR	Digital Output. Data Terminal Ready control output (active low).
24	DCD	Digital Input. Data Carrier Detect control input (active low).
Center	GND	Ground

5.3 CP2102N QFN20 Pin Definitions

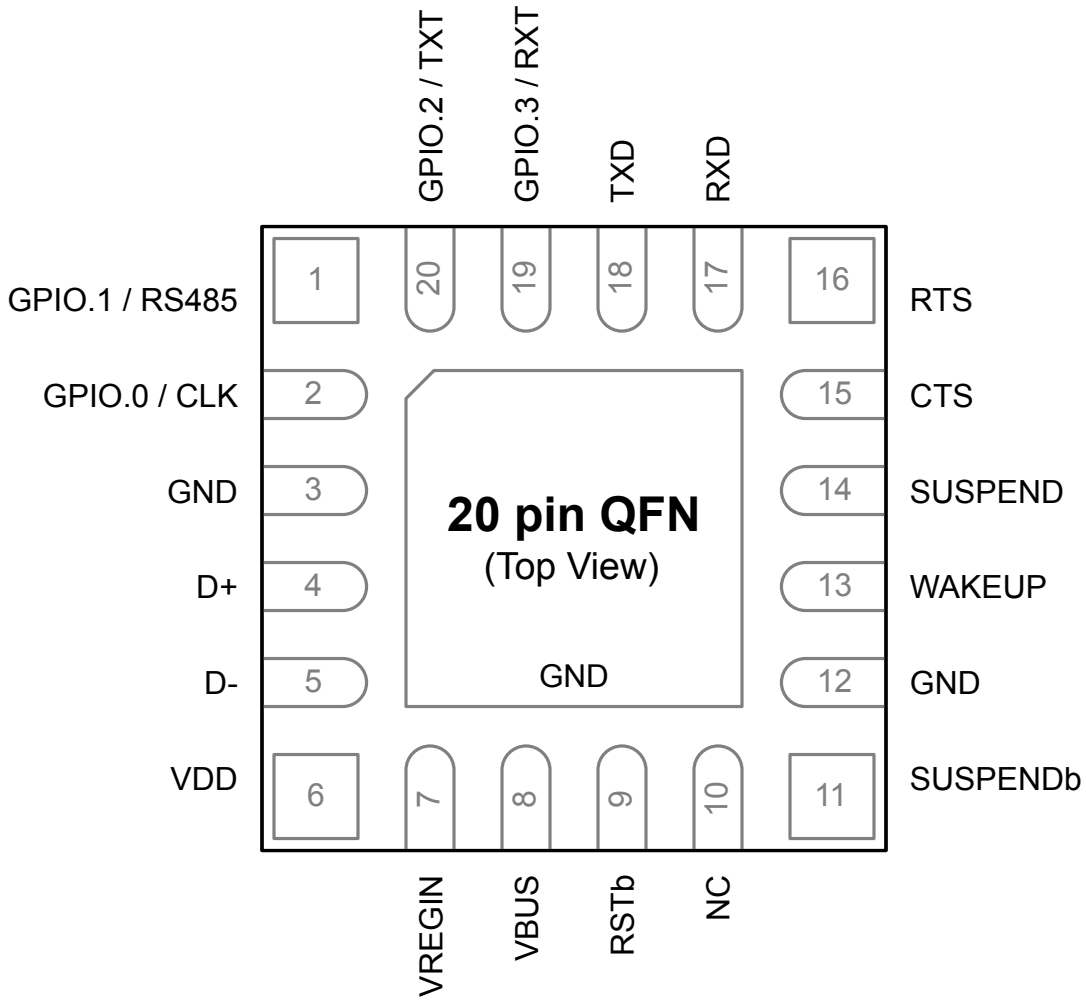


Figure 5.3. CP2102N QFN20 Pinout

Table 5.3. Pin Definitions for CP2102N QFN20

Pin Number	Pin Name	Description
1	GPIO.1 / RS485	Digital Input/Output. General Purpose I/O. Digital Output. RS485 control signal.
2	GPIO.0 / CLK	Digital Input/Output. General Purpose I/O. Digital Output. Clock output.
3	GND	Ground
4	D+	USB Data Positive
5	D-	USB Data Negative

Pin Number	Pin Name	Description
6	VDD	Supply Power Input / 5V Regulator Output
7	VREGIN	5V Regulator Input
8	VBUS	Digital Input. VBUS Sense Input. This pin should be connected to the VBUS signal of a USB network. A 5 V signal on this pin indicates a USB network connection.
9	RSTb	Active-low Reset
10	NC	No Connect (leave this pin floating).
11	SUSPENDb	Digital Output. This pin is driven low when the device enters the USB suspend state.
12	GND	Ground
13	WAKEUP	Digital Input. Remote USB wakeup interrupt input.
14	SUSPEND	Digital Output. This pin is driven high when the device enters the USB suspend state.
15	CTS	Digital Input. Clear To Send control input (active low).
16	RTS	Digital Output. Ready To Send control output (active low).
17	RXD	Digital Input. Asynchronous data input (UART Receive).
18	TXD	Digital Output. Asynchronous data output (UART Transmit).
19	GPIO.3 / RXT	Digital Input/Output. General Purpose I/O. Digital Output. Receive LED toggle.
20	GPIO.2 / TXT	Digital Input/Output. General Purpose I/O. Digital Output. Transmit LED toggle.
Center	GND	Ground

6. QFN28 Package Specifications

6.1 QFN28 Package Dimensions

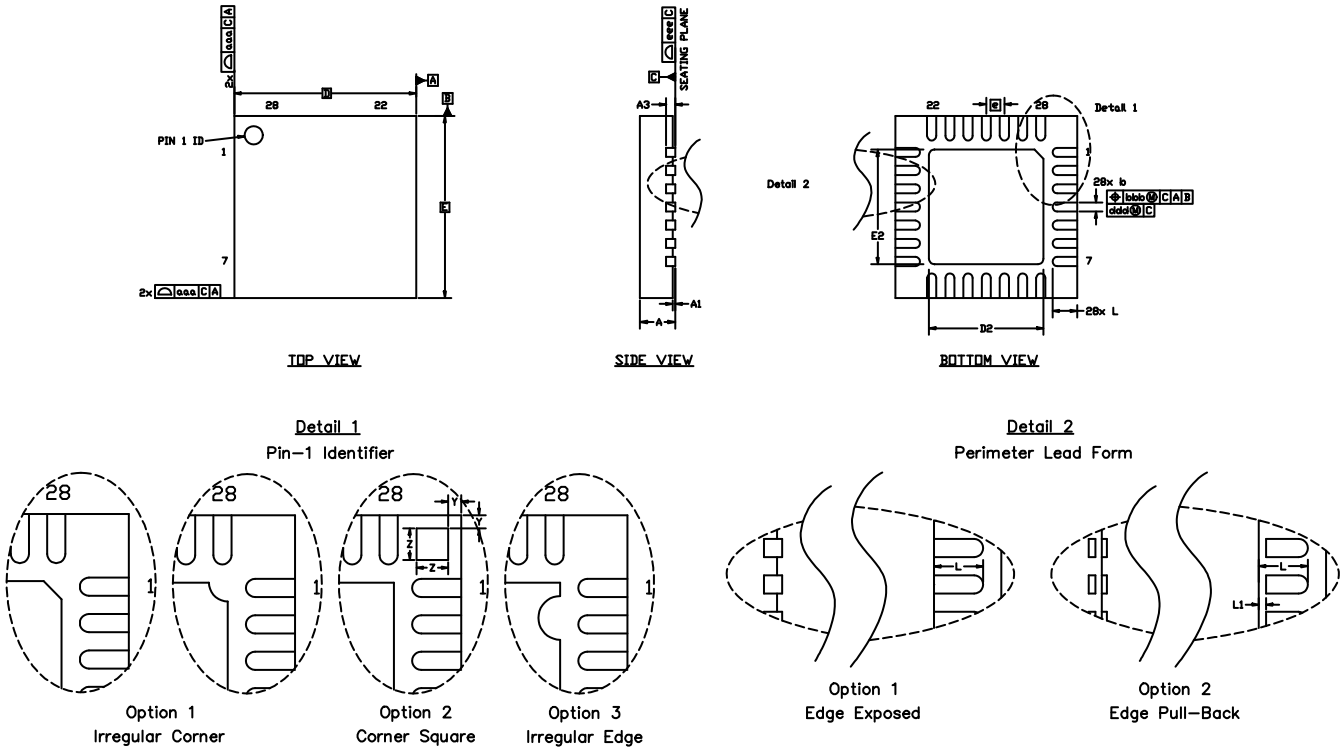


Figure 6.1. QFN28 Package Drawing

Table 6.1. QFN28 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3		0.20 REF	
b	0.20	0.25	0.30
D		5.00 BSC	
D2	3.15	3.25	3.35
e		0.50 BSC	
E		5.00 BSC	
E2	3.15	3.25	3.35
L	0.45	0.55	0.65
aaa		0.10	
bbb		0.10	
ddd		0.05	

Dimension	Min	Typ	Max
eee		0.08	
Z		0.44	
Y		0.18	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220 except for custom features D2, E2, L, Z, and Y which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.2 QFN28 PCB Land Pattern

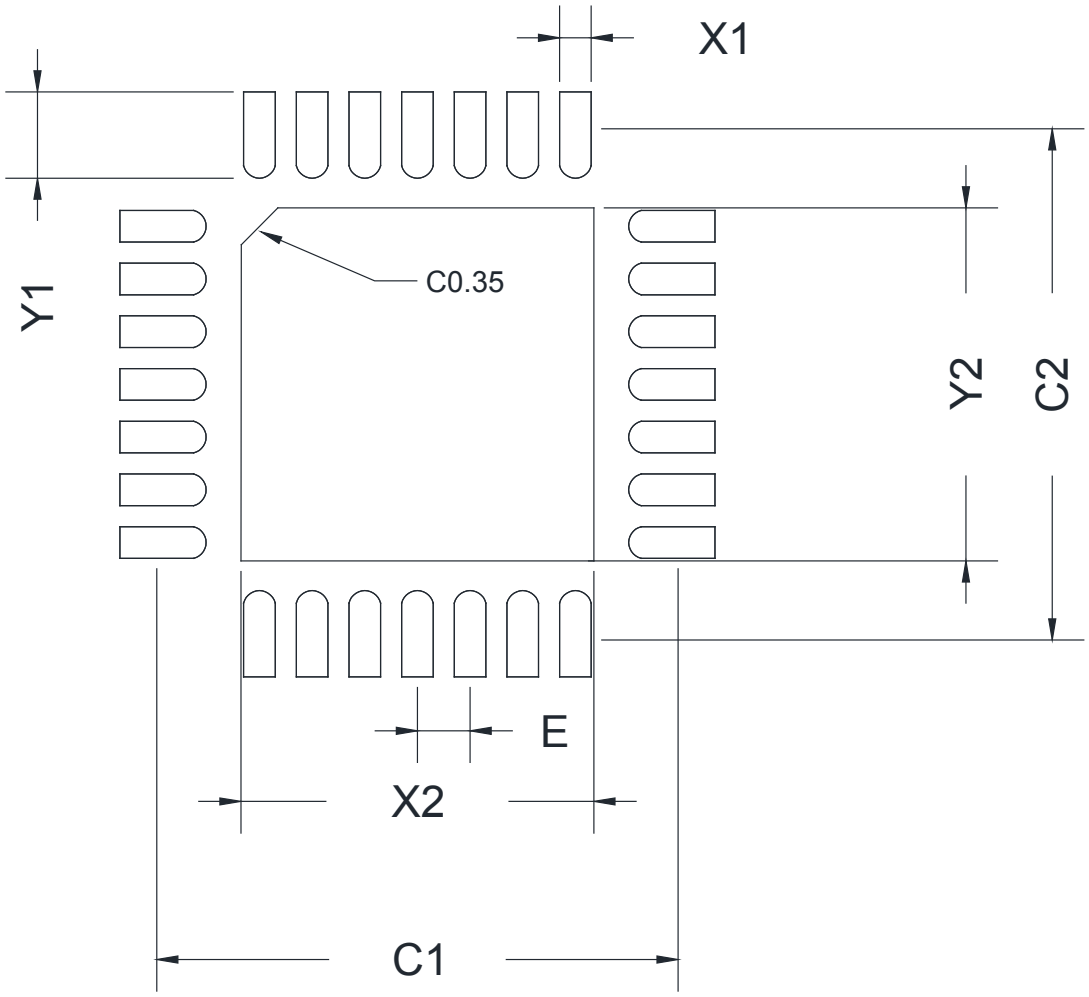


Figure 6.2. QFN28 PCB Land Pattern Drawing

Table 6.2. QFN28 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	4.80	
C2	4.80	
E	0.50	
X1	0.30	
X2	3.35	
Y1	0.95	
Y2	3.35	

Dimension	Min	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2 x 2 array of 1.2 mm square openings on a 1.5 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.3 QFN28 Package Marking

Figure 6.3. QFN28 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last two digits of the assembly year.
- WW – The two-digit workweek when the device was assembled.
- # – Indicates the hardware revision.

Note: Firmware revision is not part of the package marking.

7. QFN24 Package Specifications

7.1 QFN24 Package Dimensions

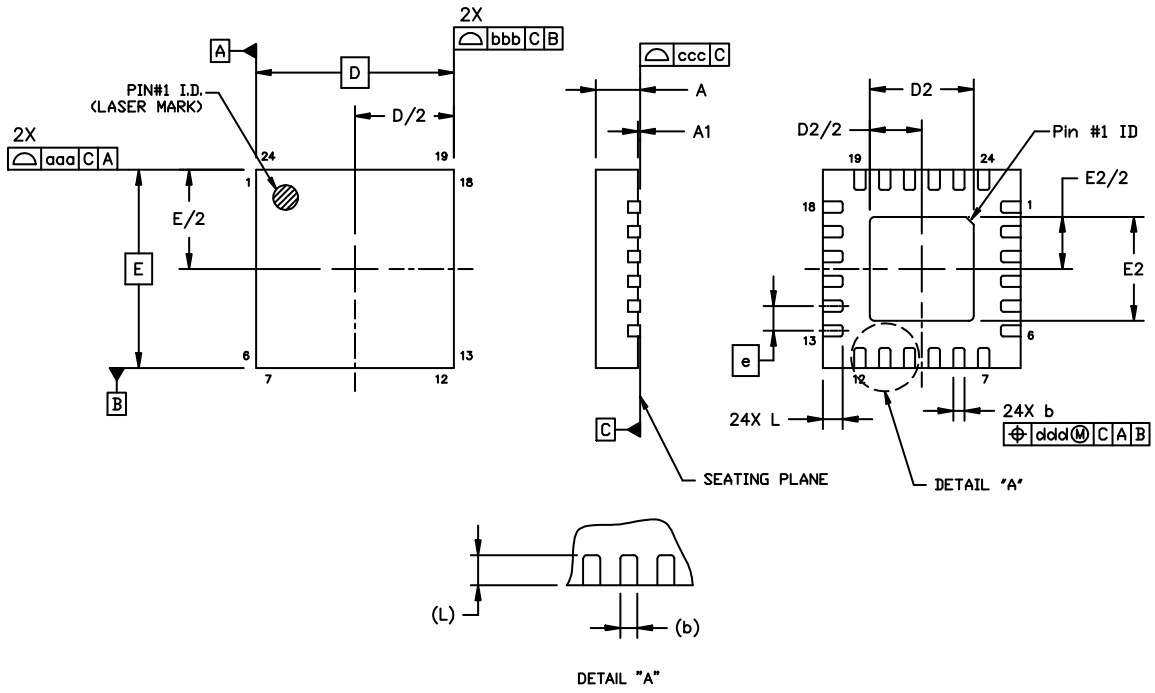


Figure 7.1. QFN24 Package Drawing

Table 7.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.18	0.25	0.30
D		4.00 BSC	
D2	2.35	2.45	2.55
e		0.50 BSC	
E		4.00 BSC	
E2	2.35	2.45	2.55
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Dimension	Min	Typ	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.2 PCB Land Pattern

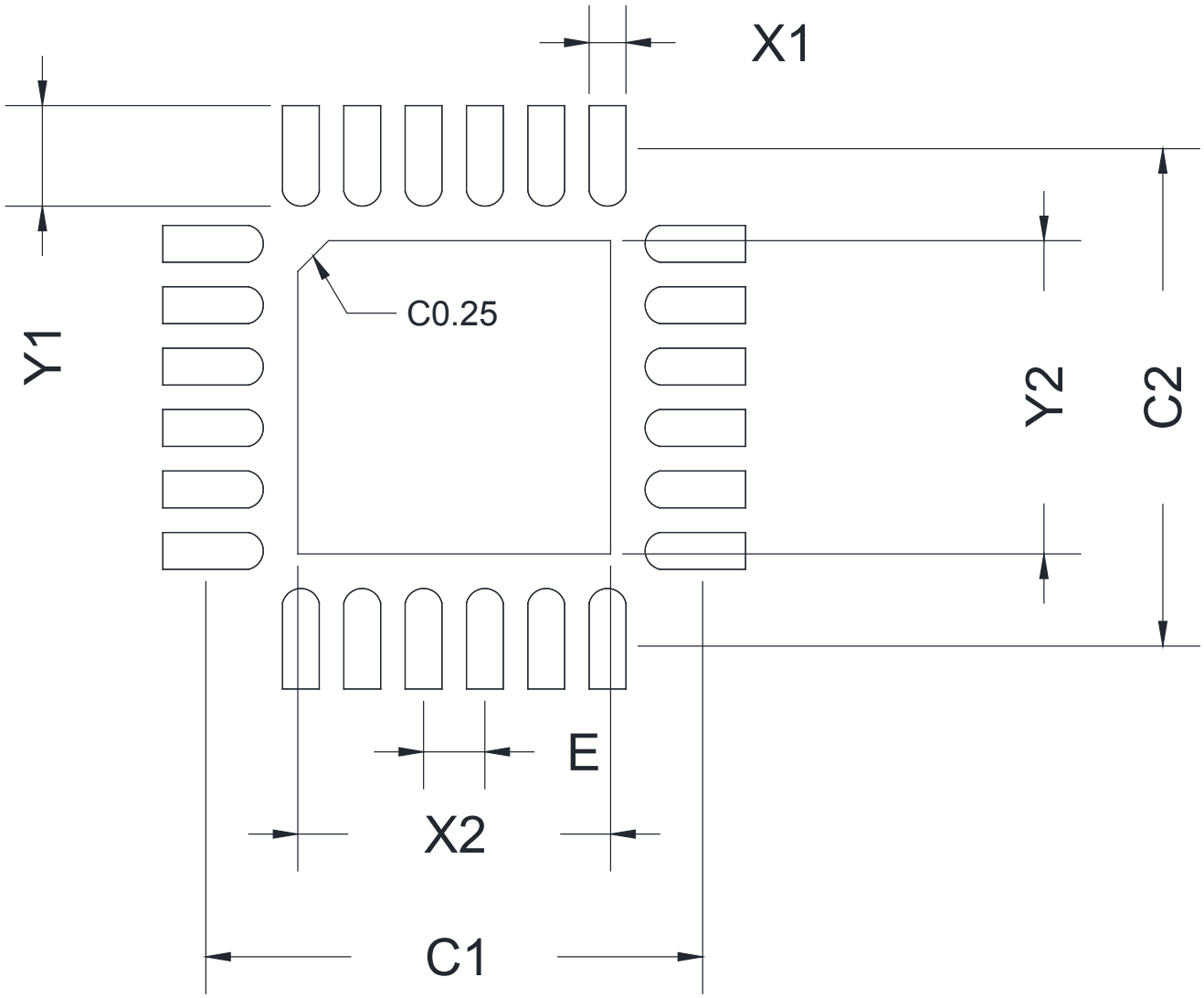


Figure 7.2. PCB Land Pattern Drawing

Table 7.2. PCB Land Pattern Dimensions

Dimension	Min	Max
C1	3.90	
C2	3.90	
E	0.50	
X1	0.30	
X2	2.55	
Y1	0.85	
Y2	2.55	

Dimension	Min	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2 x 2 array of 0.9 mm square openings on a 1.2 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 Package Marking

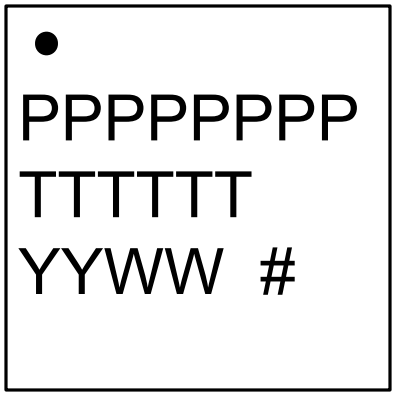


Figure 7.3. Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last two digits of the assembly year.
- WW – The two-digit workweek when the device was assembled.
- # – Indicates the hardware revision.

Note: Firmware revision is not part of the package marking.

8. QFN20 Package Specifications

8.1 QFN20 Package Dimensions

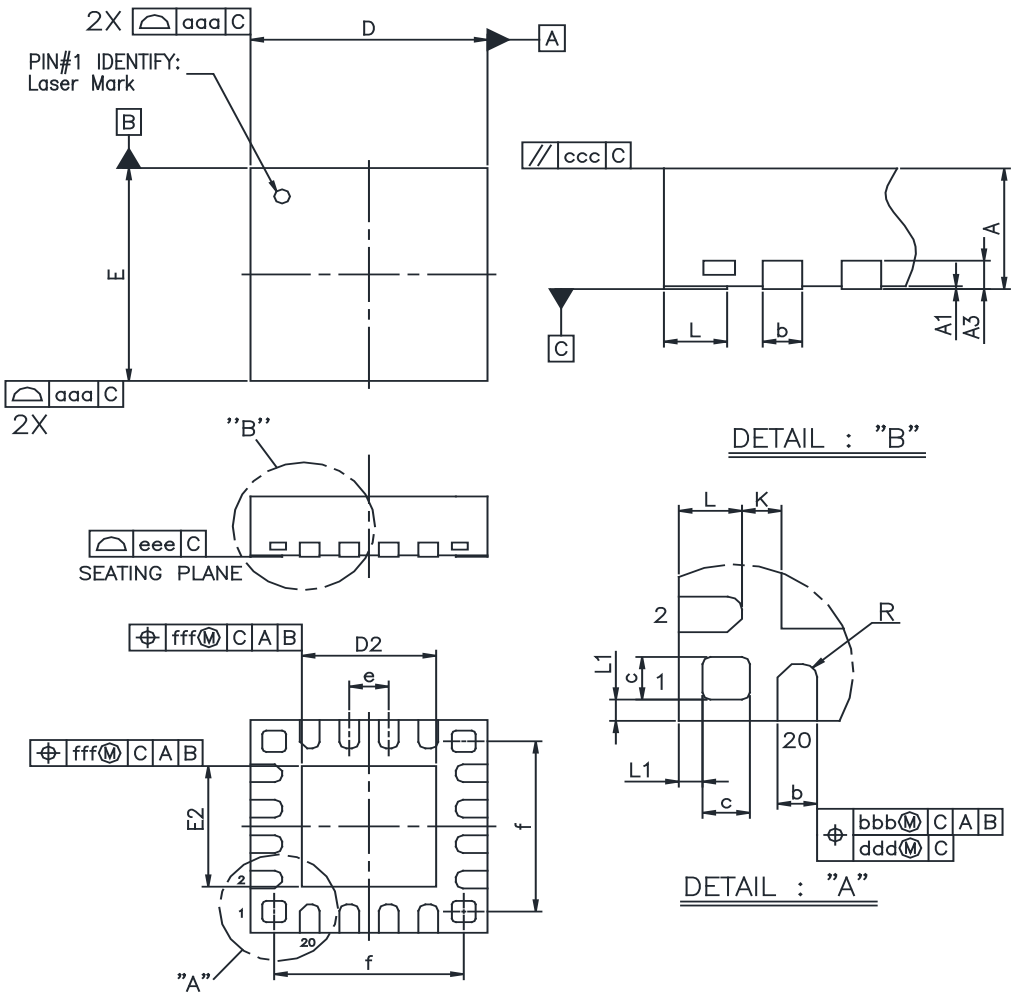


Figure 8.1. QFN20 Package Drawing

Table 8.1. QFN20 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
c	0.25	0.30	0.35
D		3.00 BSC	
D2	1.6	1.70	1.80
e		0.50 BSC	
E		3.00 BSC	

Dimension	Min	Typ	Max
E2	1.60	1.70	1.80
f		2.50 BSC	
L	0.30	0.40	0.50
K		0.25 REF	
R	0.09	0.125	0.15
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. The drawing complies with JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 QFN20 PCB Land Pattern

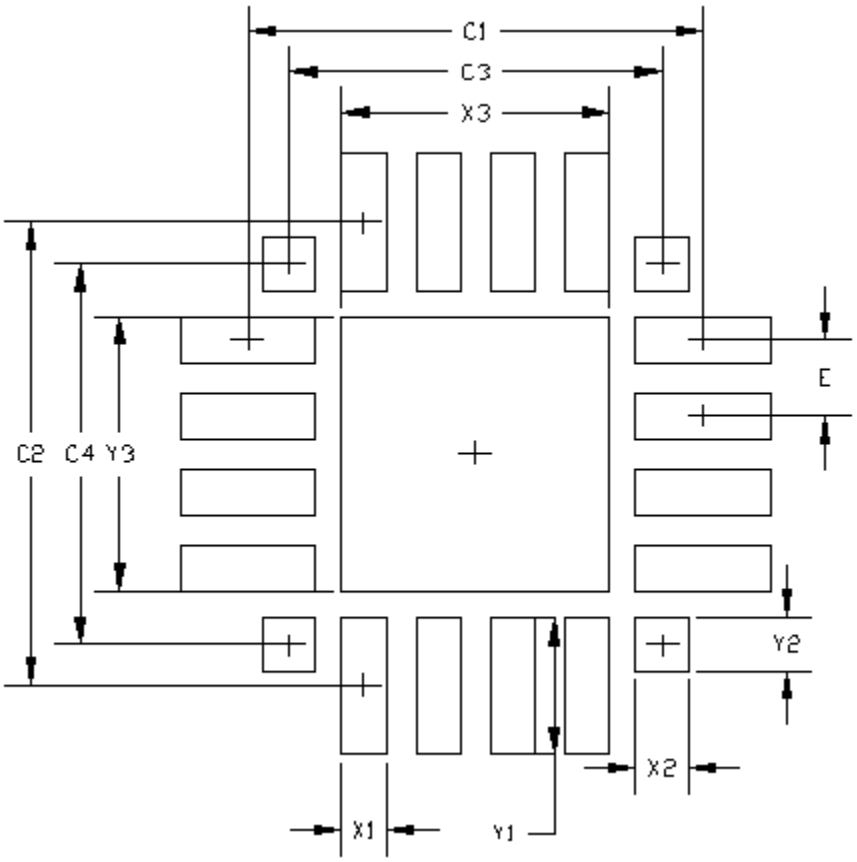


Figure 8.2. QFN20 PCB Land Pattern Drawing

Table 8.2. QFN20 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	3.10	
C2	3.10	
C3	2.50	
C4	2.50	
E	0.50	
X1	0.30	
X2	0.25	0.35
X3	1.80	
Y1	0.90	
Y2	0.25	0.35
Y3	1.80	

Dimension	Min	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
8. A 2 x 2 array of 0.75 mm openings on a 0.95 mm pitch should be used for the center pad to assure proper paste volume.
9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.3 QFN20 Package Marking

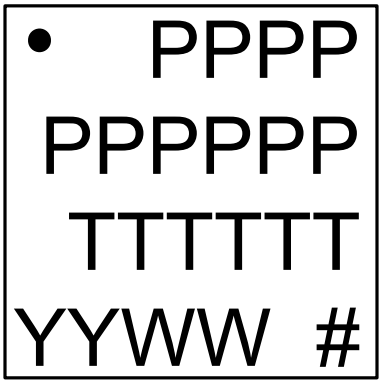


Figure 8.3. QFN20 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- Y – The last digit of the assembly year.
- WW – The two-digit workweek when the device was assembled.
- # – Indicates the hardware revision.

Note: Firmware revision is not part of the package marking.

9. Relevant Application Notes

The following Application Notes are applicable to the CP2102N devices:

- *AN721: CP210x Device Customization Guide* — This application note guides developers through the configuration process of USBXpress devices using Simplicity Studio [**Xpress Configurator**].
- *AN220: USB Driver Customization* — This document and accompanying software enable the customization of the CP210x Virtual COM Port (VCP) and USBXpress drivers.
- *AN197: Serial Communications Guide for CP210x* — This document describes recommendations for communicating with USBXpress CP210x devices using the Virtual COM Port (VCP) driver.
- *AN976: Migrating from a CP2102 to a CP2102N* — This document guides developers on how to migrate existing systems using the CP2102 to the CP2102N.
- *AN169: USBXpress Programmer's Guide* — This application note provides recommendations and examples for developing using the USBXpress direct-access driver.
- *AN807: Recertifying a Customized Windows HCK Driver Package* — This document describes the WHQL certification process required for customized drivers.
- *AN223: Runtime GPIO Control for CP210x* — This document describes how to toggle GPIO pins from the USB host.

Application Notes can be accessed on the Silicon Labs website (www.silabs.com/interface-appnotes) or in Simplicity Studio using the [**Application Notes**] tile.

10. Revision History

Revision 1.5

November, 2020

- Updated Figure 2.6 Self-Powered Connection Diagram for USB Pins on page 9 to add back VBUS voltage divider that was accidentally removed in previous revision.

Revision 1.4

October, 2020

- Updated Figure 2.4 Battery Charging Connection Diagram on page 7, Figure 2.5 Bus-Powered Connection Diagram for USB Pins on page 8, and Figure 2.6 Self-Powered Connection Diagram for USB Pins on page 9 to reflect new SP0503BAHTG protection device RoHS-compliant part number.
- Added firmware note to the package marking sections.

Revision 1.3

March, 2019

- Updated Table 1.1 Product Selection Guide on page 2 to reflect revison change to CP2102N-A02 devices.
- Added section 4.2.2 Sending Break Signaling describing how to send line breaks
- Added section 4.3.13 Receiver Timeout describing the new custom vendor command to configure the internal buffer receive timeout
- Changed note in 4.3.12 RS485 (RS485) to indicate that in CP2102N-A02, the RS485 pin is not available at baud rates below 300 baud.
- Changed information in 4.3.8 Software Handshaking to indicate that in CP2102N-A02, watermark levels greater than 512 are converted to an XON limit of 192 and an XOFF limit of 64 bytes.
- Updated PCB land pattern diagram in 8.2 QFN20 PCB Land Pattern.

Revision 1.2

November, 2017

- Added a note to Table 1.1 Product Selection Guide on page 2 to clarify the multiple types of pin 1 indicators for each package.
- Added a description of the RSTb pin behavior during reset to 2.1 Power and as a note on 3.1.3 Reset and Supply Monitor.
- Updated the note regarding the resistor divider on VBUS, added the resistor divider to Figure 2.5 Bus-Powered Connection Diagram for USB Pins on page 8, and duplicated the note to this area in 2.3 USB.
- Added the resistor divider on VBUS to Figure 2.4 Battery Charging Connection Diagram on page 7.
- Updated Thermal Resistance to Thermal Resistance (Junction to Ambient) and added Thermal Resistance (Junction to Case) and Thermal Characterization Parameter (Junction to Top) for all packages to 3.2 Thermal Conditions.
- Updated 4.3.4 Battery Charging (CHREN, CHR0, and CHR1) to include information about configuring GPIO for battery charging.
- Updated 4.3.7 Hardware Handshaking (RTS and CTS) and 4.3.12 RS485 (RS485) with a note that RTS control signaling and RS485 features are not supported below 1200 baud.
- Added Z and Y dimensions and updated Note 3 in Table 6.1 QFN28 Package Dimensions on page 33.
- Updated revision history format and moved table of contents.

Revision 1.1

August, 2016

- Updated the minimum Operating Supply Voltage on VDD to 3.0 V in 1. Feature List and Ordering Information, 3.1.1 Recommended Operating Conditions, 3.1.4 Configuration Memory, and Figure 2.3 Connection Diagram with Voltage Regulator Not Used on page 6.
- Updated 4.3.6 Clock Output (CLK) to specify that the clock is not present when the device is in USB Suspend.
- Updated QFN24 bottom pad label to GND instead of VSS.
- Adjusted D, E, and aaa in QFN28 Package Dimensions.
- Adjusted D, E, and L in QFN24 Package Dimensions.

Revision 1.0

May, 2016

- Initial release.

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