BGM11S Blue Gecko *Bluetooth*® SiP 模块数据表

BGM11S Blue Gecko *Bluetooth*® SiP 模块 产品系列致力于满足用户对于超小体积、卓越 RF 性能、低功耗和轻松开发应用的关键需求。

BGM11S 模块大小为 6.5 x 6.5 x 1.4 mm，适用于体积受限的应用。同时，BGM11S 也整合了高性能且非常可靠的天线，这需要 PCB、塑料与金属的净空达到最小。BGM11S 所需的 PCB 总面积仅为 51 mm^2。BGM11S 已获 Bluetooth、CE、完整 FCC、加拿大 ISED、日本、韩国和中国台湾认证。

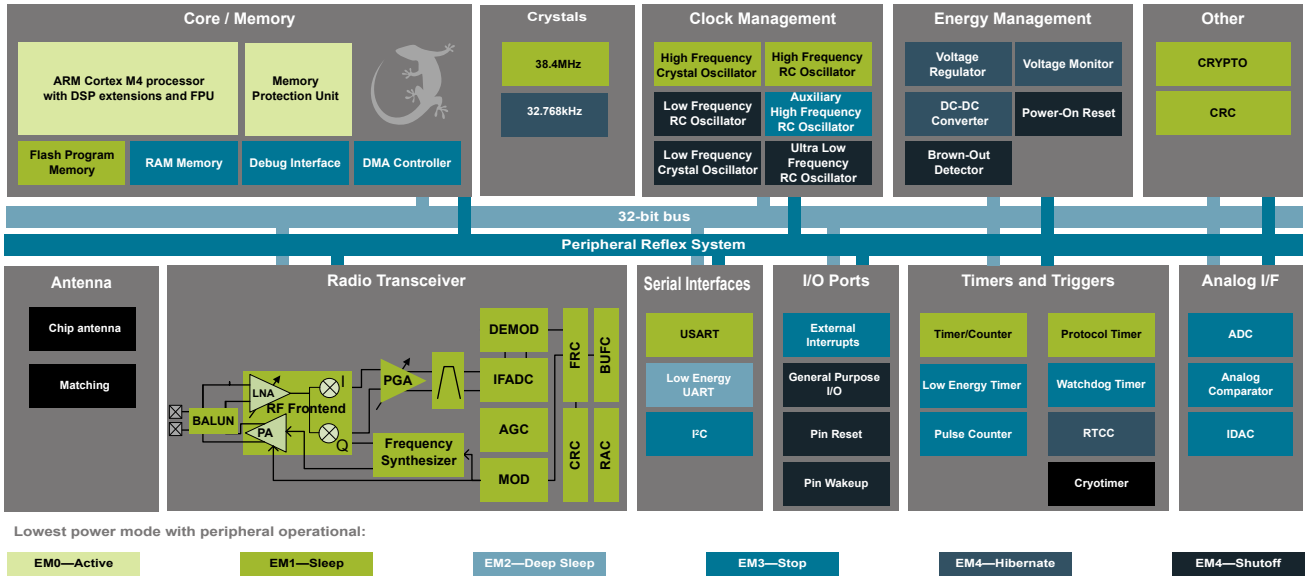
BGM11S 基于 EFR32BG1 SoC，还整合了符合 *Bluetooth* 4.2 标准的 Bluetooth 低功耗技术，可运行板载终端用户应用或作为主机接口之一的网络协同处理器进行使用。

BGM11S SIP 模块可用于广泛的应用中：

- 可穿戴产品
- IoT 终端设备和网关
- 医疗、运动和健康设备
- 工业、家庭和楼宇自动化
- 智能手机、平板电脑和台式电脑配件
- 信标

主要特点

- Bluetooth 4.2 低功耗合规
- 集成天线或 RF 引脚
- TX 功率高达 +8 dBm
- RX 灵敏度：-90 dBm
- 距离：长达 200 米
- 32 位 ARM® Cortex®-M4 内核为 38.4 MHz
- 闪存：256 kB
- RAM：32 kB
- 自主硬件加密加速器和随机数生成器
- 集成直流转换器
- 板载 Bluetooth 协议栈



1. 功能列表

BGM11S 突出功能如下所列。

- **低功耗无线片上系统**。
  - 高性能 32 位 38.4 MHz ARM Cortex®-M4，带有 DSP 指令和浮点单元，可实现高效的信号处理
  - 256 kB 闪存程序存储器
  - 32 kB RAM 数据存储器
  - 2.4 GHz 无线电操作
  - TX 功率高达 +8 dBm
- **低能耗**
  - 在 2.4 GHz 时，RX 电流为 8.7 mA
  - 在 2.4 GHz 时，0 dBm 输出功率下的 TX 电流为 8.2 mA
  - 在活动模式 (EM0) 下，运行功耗为 63 µA/MHz
  - 2.5 µA EM2 深度睡眠电流（保留全部 RAM，RTCC 从 LFXO 中运行）
  - 2.1 µA EM3 停止电流（状态/RAM 保留）
- **接收器性能高**
  - 在 2.4 GHz、1 Mbit/s GFSK 的条件下，灵敏度为

    -90 dBm
- **支持的协议**
  - Bluetooth® 低能耗
- **互联网安全支持**
  - 通用 CRC
  - 随机数生成器
  - 硬件加密加速器，支持 AES 128/256、SHA-1、SHA-2（SHA-224 和 SHA-256）和 ECC
- **广泛的 MCU 外围设备选择**
  - 12 位 1 Msps SAR 模拟数字转换器 (ADC)
  - 2 个模拟比较器 (ACMP)
  - 数字模拟电流转换器 (IDAC)
  - 32 个引脚连接到模拟比较器、ADC 和 IDAC 之间共享的模拟通道 (APORT)
  - 30 个带有输出状态保持和异步中断功能的通用 I/O 引脚
  - 8 信道 DMA 控制器
  - 12 信道外围设备反射系统 (PRS)
  - 2 个 16 位定时器/计数器
    - 3 + 4 比较/捕获/PWM 通道
  - 32 位实时计数器和日历
  - 16 位低能耗定时器，用于波形生成
  - 32 位超低能耗定时器/计数器，用于任何能源模式的定期唤醒
  - 16 位脉冲计数器，带有异步操作
  - 带专用 RC 振荡器的看门狗定时器（电流为 50 nA 时）
  - 2 个通用同步/异步接收器/传输器 (UART/SPI/SmartCard (ISO 7816)/IrDA/I^2S)
  - 低功耗 UART (LEUART™)
  - I^2C 接口，带有 SMBus 支持和 EM3 停止模式下的地址识别
- **宽工作范围**
  - 1.85 至 3.8 V 单电源
  - 使用 DC-DC 时为 2.4 V 至 3.8 V
  - 集成 DC-DC
  - –40 °C 至 +85 °C
- **尺寸**
  - 6.5 x 6.5 x 1.4 mm

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Protocol Stack	Frequency Band	Max TX Power (dBm)	Antenna	Flash (KB)	RAM (KB)	GPIO	Package
BGM11S12F256GA-V2R	Bluetooth® Low Energy	2.4 GHz	+2	Built-in	256	32	30	1000 pcs reel
BGM11S12F256GA-V2	Bluetooth® Low Energy	2.4 GHz	+2	Built-in	256	32	30	260 pcs tray
BGM11S22F256GA-V2R	Bluetooth ® Low Energy	2.4 GHz	+8	Built-in	256	32	30	1000 pcs reel
BGM11S22F256GA-V2	Bluetooth® Low Energy	2.4 GHz	+8	Built-in	256	32	30	260 pcs tray
SLWSTK6101C[1]								
SLWRB4303A[2]								

Note:

1. Blue Gecko Bluetooth Module Wireless Starter Kit (WSTK) with BGM121A256 radio board (SLWRB4302A) and BGM111A256 radio board (SLWRB4300A), expansion board and accessories.
2. BGM11S22F256GA-V2 Radio Board

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3. System Overview

3.1 Introduction

The BGM11S product family combines an energy-friendly MCU with a highly integrated radio transceiver. The devices are well suited for any battery operated application, as well as other system requiring high performance and low-energy consumption. This section gives a short introduction to the full radio and MCU system. A detailed functional description can be found in the *EFR32BG1 Wireless Gecko Bluetooth® Low Energy SoC Family Data Sheet* (see general sections and QFN48 2.4 GHz SoC related sections).

A detailed block diagram of the EFR32BG SoC is shown in the figure below which is used in the BGM11S Bluetooth Low Energy module.

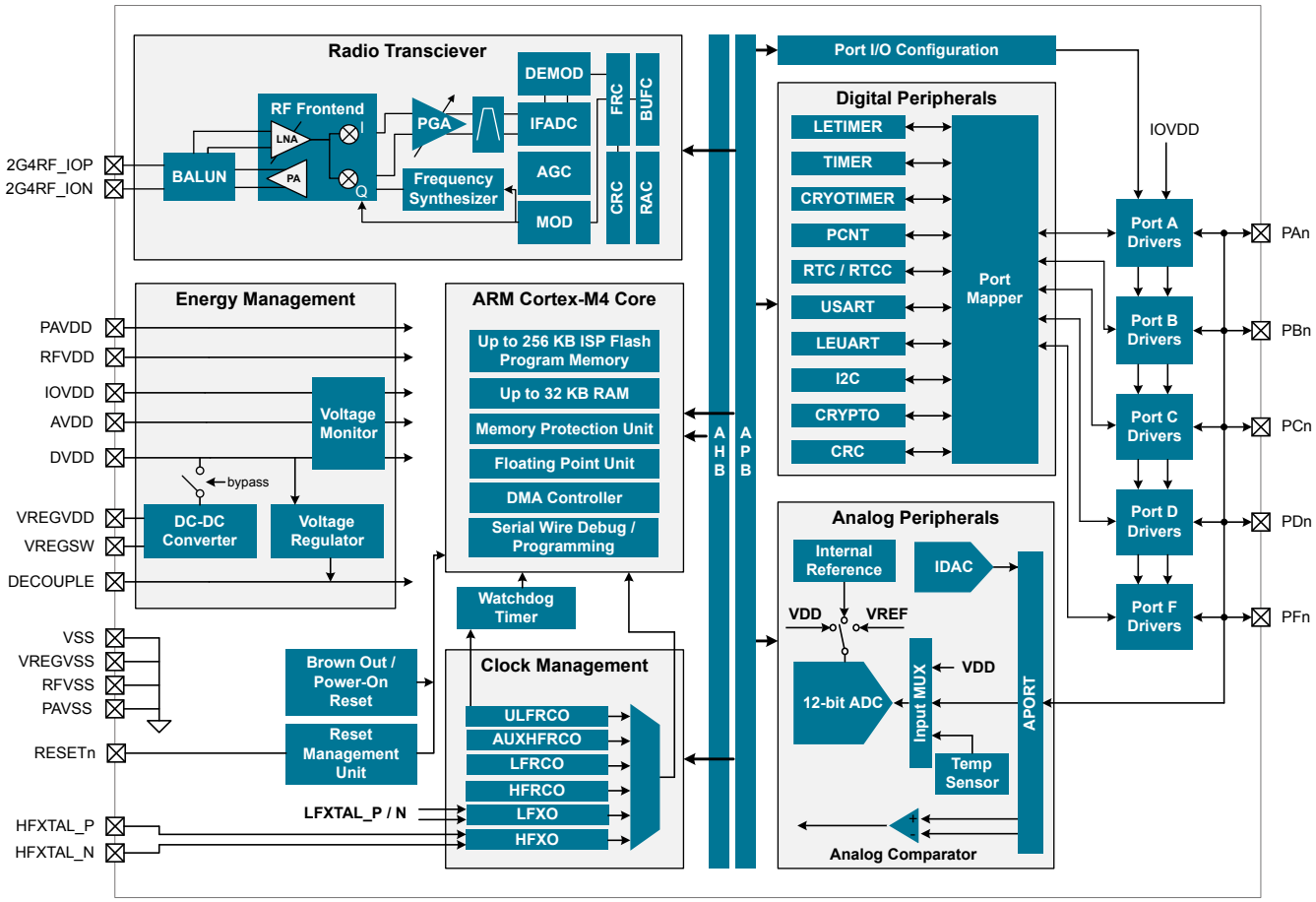


Figure 3.1. Detailed EFR32BG1 Block Diagram

3.2 Radio

The BGM11S features a radio transceiver supporting Bluetooth® low energy protocol.

3.2.1 Antenna Interface

BGM11S has a built in 2.4GHz ceramic chip antenna or 50 ohm RF pin.

Table 3.1. Antenna Efficiency and Peak Gain

Parameter	With optimal layout	Note
Efficiency	-1 to -2 dB	Efficiency and peak gain depend on the application PCB layout and mechanical design and the used antenna.
Peak gain	1 dBi	

3.2.2 Packet and State Trace

The BGM11S Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.2.3 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.

3.3 Power

The BGM11S has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An integrated dc-dc buck regulator is utilized to further reduce the current consumption.

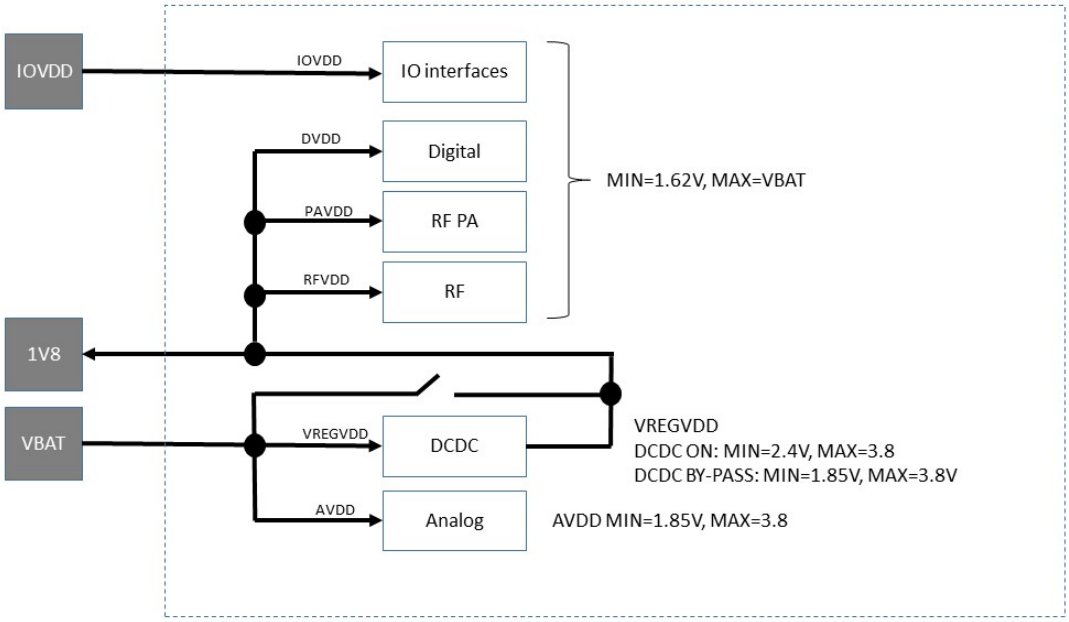


Figure 3.2. Power Supply Configuration

3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the dc-dc regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.3.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3. Patented RF noise mitigation allows operation of the DC-DC converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.4 General Purpose Input/Output (GPIO)

BGM11S has up to 30 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.5 Clocking

3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the BGM11S. Individual enabling and disabling of clocks to all peripheral modules is perfomed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.5.2 Internal Oscillators

The BGM11S fully integrates two crystal oscillators and four RC oscillators, listed below.

- A 38.4MHz high frequency crystal oscillator (HFXO) provides a precise timing reference for the MCU and radio.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire debug port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.6 Counters/Timers and PWM

3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.6.2 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes.

3.6.3 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.6.4 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.6.5 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.6.6 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.7 Communications and Other Digital Peripherals

3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™ provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.7.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality can be applied by the PRS. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.8 Security Features

3.8.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. It supports AES encryption and decryption with 128- or 256-bit keys and ECC over both GF(P) and GF(2^m), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.9 Analog

3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to analog modules ADC, ACMP, and IDAC on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 MSamples/s. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.9.4 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The current is programmable between 0.05 µA and 64 µA with several ranges with various step sizes.

3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the BGM11S. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset and watchdog reset.

3.11 Core and Memory

3.11.1 Processor Core

The ARM Cortex-M4F processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4F RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- 256 KB flash program memory
- 32 KB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller features 8 channels capable of performing memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12 Memory Map

The BGM11S memory map is shown in the figures below.

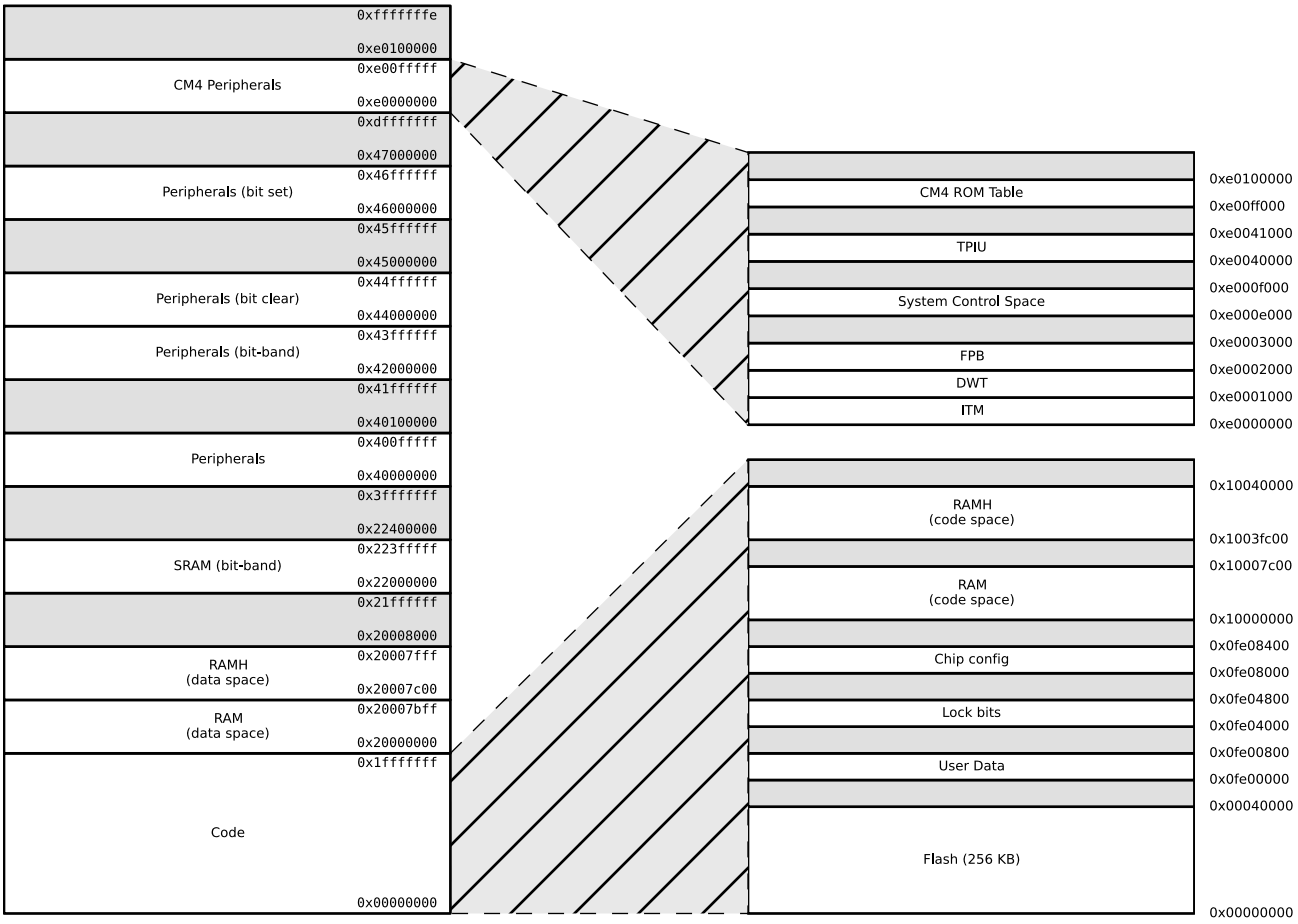


Figure 3.3. BGM11S Memory Map — Core Peripherals and Code Space

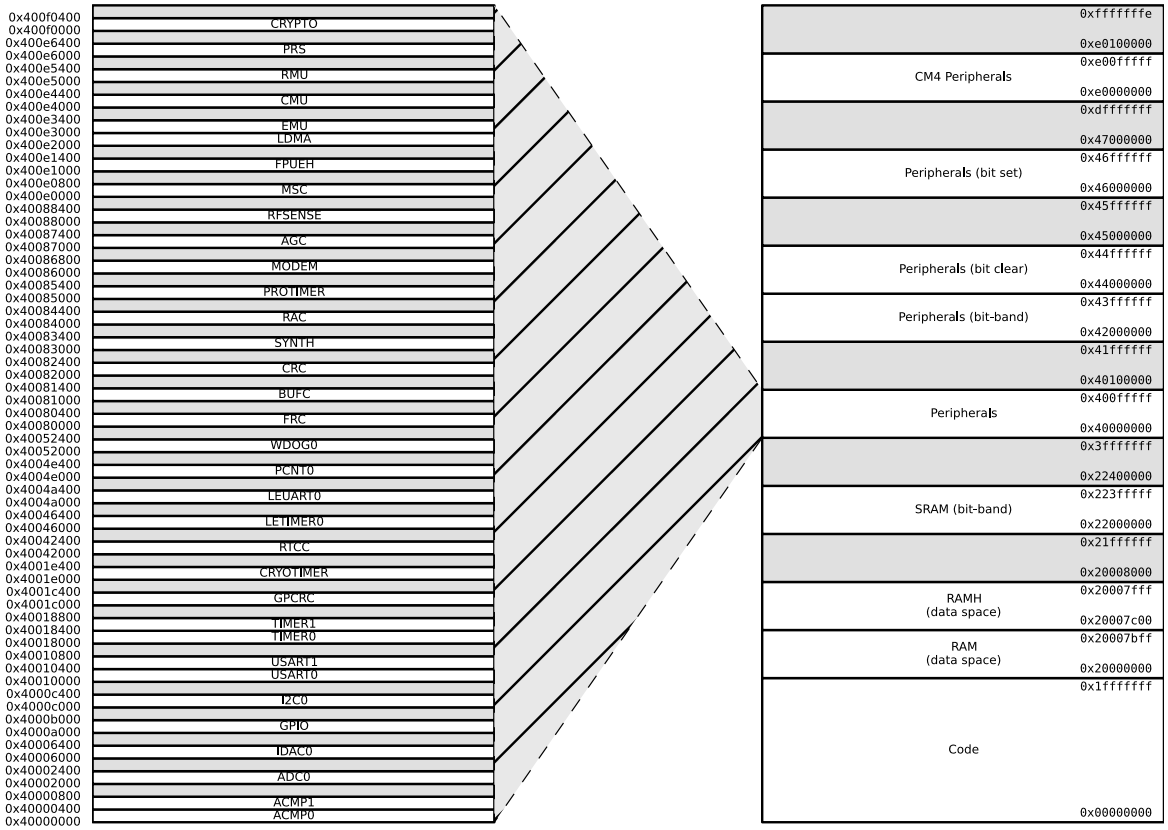


Figure 3.4. BGM11S Memory Map — Peripherals

3.13 Configuration Summary

The features of the BGM11S are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.2. Configuration Summary

Module	Configuration	Pin Connections
USART0	IrDA SmartCard	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	IrDA I^2S SmartCard	US1_TX, US1_RX, US1_CLK, US1_CS
TIMER0	with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1		TIM1_CC[3:0]

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_{AMB}=25 °C and V_{DD}= 3.3 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to Table 4.2 General Operating Conditions on page 17 for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-40	—	+85	°C
External main supply voltage	V_{DDMAX}		0	—	3.8	V
External main supply voltage ramp rate	$V_{DDRAMPMAX}$		—	—	1	V / µs
External main supply voltage with DC-DC in bypass mode			1.85		3.8	V
Voltage on any 5V tolerant GPIO pin[1]	V_{DIGPIN}		-0.3	—	Min of 5.25 and IOVDD +2	V
Voltage on non-5V tolerant GPIO pins			-0.3	—	IOVDD+0.3	V
Max RF level at input	$P_{RFMAX2G4}$		—	—	10	dBm
Total current into VDD power lines (source)	I_{VDDMAX}		—	—	200	mA
Total current into VSS ground lines (sink)	I_{VSSMAX}		—	—	200	mA
Current per I/O pin (sink)	I_{IOMAX}		—	—	50	mA
Current per I/O pin (source)			—	—	50	mA
Current for all I/O pins (sink)	$I_{IOALLMAX}$		—	—	200	mA
Current for all I/O pins (source)			—	—	200	mA
Voltage difference between AVDD and VREGVDD	ΔV_{DD}		—	—	0.3	V

Note:

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.

4.1.2 Operating Conditions

The following subsections define the operating conditions for the module.

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating temperature range	T_{OP}	Ambient temperature range	-40	25	85	°C
VDD Operating supply voltage [1]	V_{VDD}	DCDC in regulation	2.4[3]	3.3	3.8	V
		DCDC in bypass, 50mA load	1.85	3.3	3.8	V
VDD Current	I_{VDD}	DCDC in bypass	—	—	200	mA
HFCLK frequency	f_{CORE}	0 wait-states (MODE = WS0) [2]	—	—	26	MHz
		1 wait-states (MODE = WS1) [2]	—	38.4	40	MHz

Note:

1. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DC-DC specification table. Requirements for other loads can be calculated as $V_{VDD\_min}+I_{LOAD} * R_{BYP\_max}$
2. In MSC_READCTRL register
3. The minimum voltage of 2.4 V for DCDC is specified at 100 mA

4.1.3 DC-DC Converter

Test conditions: V_{DCDC_I}=3.3 V, V_{DCDC_O}=1.8 V, I_{DCDC_LOAD}=50 mA, Heavy Drive configuration, F_{DCDC_LN}=7 MHz, unless otherwise indicated.

Table 4.3. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{DCDC_I}	Bypass mode, I_{DCDC_LOAD} = 50 mA	1.85	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I_{DCDC_LOAD} = 10 mA	2.4	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 200 mA	2.6	—	$V_{VREGVDD\_MAX}$	V
Output voltage programmable range[1]	V_{DCDC_O}		1.8	—	$V_{VREGVDD}$	V
Regulation DC Accuracy	ACC_{DC}	Low noise (LN) mode, 1.8 V target output	1.7	—	1.9	V
Regulation Window[2]	WIN_{REG}	Low power (LP) mode, LPCMPBIAS[3] = 0, 1.8 V target output, I_{DCDC_LOAD} ≤ 75 µA	1.63	—	2.2	V
		Low power (LP) mode, LPCMPBIAS[3] = 3, 1.8 V target output, I_{DCDC_LOAD} ≤ 10 mA	1.63	—	2.1	V
Steady-state output ripple	V_R	Radio disabled.	—	3	—	mVpp
Output voltage under/overshoot	V_{OV}	CCM Mode (LNFORCECCM[3] = 1), Load changes between 0 mA and 100 mA	—	—	150	mV
		DCM Mode (LNFORCECCM[3] = 0), Load changes between 0 mA and 10 mA	—	—	150	mV
		Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode	—	200	—	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM[3] = 1) mode transitions compared to DC level in LN mode	—	50	—	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM[3] = 0) mode transitions compared to DC level in LN mode	—	125	—	mV
DC line regulation	V_{REG}	Input changes between $V_{VREGVDD\_MAX}$ and 2.4 V	—	0.1	—	%
DC load regulation	I_{REG}	Load changes between 0 mA and 100 mA in CCM mode	—	0.1	—	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, $V_{VREGVDD}$
2. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits
3. In EMU_DCDCMISCCTRL register
4. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.

4.1.4 Current Consumption

4.1.4.1 Current Consumption 3.3 V (DC-DC in Bypass Mode)

Unless otherwise indicated, typical conditions are: VDD = 3.3 V. T_{OP} = 25 °C. EMU_PWRCFG_PWRCG=NODCDC. EMU_DCDCCTRL_DCDCMODE=BYPASS. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C.

Table 4.4. Current Consumption 3.3V without DC/DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with all peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash[1]	—	130	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	88	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	100	105	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	112	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	102	106	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	222	350	µA/MHz
Current consumption in EM1 Sleep mode with all peripherals disabled	I_{EM1}	38.4 MHz crystal[1]	—	65	—	µA/MHz
		38 MHz HFRCO	—	35	38	µA/MHz
		26 MHz HFRCO	—	37	41	µA/MHz
		1 MHz HFRCO	—	157	275	µA/MHz
Current consumption in EM2 Deep Sleep mode.	I_{EM2}	Full RAM retention and RTCC running from LFXO	—	3.3	—	µA
		4 kB RAM retention and RTCC running from LFRCO	—	3	6.3	µA
Current consumption in EM3 Stop mode	I_{EM3}	Full RAM retention and CRYOTIMER running from ULFRCO	—	2.8	6	µA
Current consumption in EM4H Hibernate mode	I_{EM4}	128 byte RAM retention, RTCC running from LFXO	—	1.1	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.65	—	µA
		128 byte RAM retention, no RTCC	—	0.65	1.3	µA
Current consumption in EM4S Shutoff mode	I_{EM4S}	no RAM retention, no RTCC	—	0.04	0.20	µA

Note:
1. CMU_HFXOCTRL_LOWPOWER=0

4.1.4.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VDD = 3.3V. T_{OP} = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C.

Table 4.5. Current Consumption 3.3V with DC-DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with all peripherals disabled, DCDC in Low Noise DCM mode[1].	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash[2]	—	88	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	63	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	71	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	78	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	76	—	µA/MHz
Current consumption in EM0 Active mode with all peripherals disabled, DCDC in Low Noise CCM mode[3].		38.4 MHz crystal, CPU running while loop from flash[2]	—	98	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	75	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	81	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	88	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	94	—	µA/MHz
Current consumption in EM1 Sleep mode with all peripherals disabled, DCDC in Low Noise DCM mode[1].	I_{EM1}	38.4 MHz crystal[2]	—	49	—	µA/MHz
		38 MHz HFRCO	—	32	—	µA/MHz
		26 MHz HFRCO	—	38	—	µA/MHz
Current consumption in EM1 Sleep mode with all peripherals disabled, DCDC in Low Noise CCM mode[3].		38.4 MHz crystal[2]	—	61	—	µA/MHz
		38 MHz HFRCO	—	45	—	µA/MHz
		26 MHz HFRCO	—	58	—	µA/MHz
Current consumption in EM2 Deep Sleep mode. DCDC in Low Power mode[4].	I_{EM2}	Full RAM retention and RTCC running from LFXO	—	2.5	—	µA
		4 kB RAM retention and RTCC running from LFRCO	—	2.2	—	µA
Current consumption in EM3 Stop mode	I_{EM3}	Full RAM retention and CRYOTIMER running from ULFRCO	—	2.1	—	µA
Current consumption in EM4H Hibernate mode	I_{EM4}	128 byte RAM retention, RTCC running from LFXO	—	0.86	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.58	—	µA
		128 byte RAM retention, no RTCC	—	0.58	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4S Shutoff mode	I_{EM4S}	no RAM retention, no RTCC	—	0.04	—	µA

Note:

1. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD
2. CMU_HFXOCTRL_LOWPOWER=0
3. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD
4. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPBIAS=3, LPCILIMSEL=1, ANASW=DVDD

4.1.4.3 Current Consumption 1.85 V (DC-DC in Bypass Mode)

Unless otherwise indicated, typical conditions are: VDD = 1.85 V. T_{OP} = 25 °C. DC-DC in bypass mode. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C.

Table 4.6. Current Consumption 1.85V without DC/DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with all peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash[1]	—	131	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	88	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	100	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	112	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	102	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	220	—	µA/MHz
Current consumption in EM1 Sleep mode with all peripherals disabled	I_{EM1}	38.4 MHz crystal[1]	—	65	—	µA/MHz
		38 MHz HFRCO	—	35	—	µA/MHz
		26 MHz HFRCO	—	37	—	µA/MHz
		1 MHz HFRCO	—	154	—	µA/MHz
Current consumption in EM2 Deep Sleep mode	I_{EM2}	Full RAM retention and RTCC running from LFXO	—	3.2	—	µA
		4 kB RAM retention and RTCC running from LFRCO	—	2.8	—	µA
Current consumption in EM3 Stop mode	I_{EM3}	Full RAM retention and CRYOTIMER running from ULFRCO	—	2.7	—	µA
Current consumption in EM4H Hibernate mode	I_{EM4}	128 byte RAM retention, RTCC running from LFXO	—	1	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.62	—	µA
		128 byte RAM retention, no RTCC	—	0.62	—	µA
Current consumption in EM4S Shutoff mode	I_{EM4S}	No RAM retention, no RTCC	—	0.02	—	µA

Note:
1. CMU_HFXOCTRL_LOWPOWER=0

4.1.4.4 Current Consumption Using Radio

Unless otherwise indicated, typical conditions are: VDD = 3.3 V. T_{OP} = 25 °C. DC-DC on. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C.

Table 4.7. Current Consumption Using Radio 3.3 V with DC-DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled)	I_{RX}	1 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	9.0	—	mA
Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled)	I_{TX}	F = 2.4 GHz, CW, 0 dBm output power, Radio clock prescaled by 3	—	8.2	—	mA
		F = 2.4 GHz, CW, 2 dBm output power	—	16.5	—	mA
		F = 2.4 GHz, CW, 8 dBm output power	—	24.6	—	mA

4.1.5 Wake up times

Table 4.8. Wake up times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake up from EM2 Deep Sleep	t_{EM2_WU}	Code execution from flash	—	10.7	—	µs
		Code execution from RAM	—	3	—	µs
Wakeup time from EM1 Sleep	t_{EM1_WU}	Executing from flash	—	3	—	AHB Clocks
		Executing from RAM	—	3	—	AHB Clocks
Wake up from EM3 Stop	t_{EM3_WU}	Executing from flash	—	10.7	—	µs
		Executing from RAM	—	3	—	µs
Wake up from EM4H Hibernate[1]	t_{EM4H_WU}	Executing from flash	—	60	—	µs
Wake up from EM4S Shutoff[1]	t_{EM4S_WU}		—	290	—	µs

Note:
1. Time from wakeup request until first instruction is executed. Wakeup results in device reset.

4.1.6 Brown Out Detector

For the table below, see Figure 3.2 Power Supply Configuration on page 9 on page 5 to see the relation between the modules external VDD pin and internal voltage supplies. The module itself has only one external power supply input (VDD).

Table 4.9. Brown Out Detector

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AVDD BOD threshold	$V_{AVDDBOD}$	AVDD rising	—	—	1.85	V
		AVDD falling	1.62	—	—	V
AVDD BOD hysteresis	$V_{AVDDBOD\_HYST}$		—	21	—	mV
AVDD response time	$t_{AVDDBOD\_DELAY}$	Supply drops at 0.1V/µs rate	—	2.4	—	µs
EM4 BOD threshold	$V_{EM4DBOD}$	AVDD rising	—	—	1.7	V
		AVDD falling	1.45	—	—	V
EM4 BOD hysteresis	V_{EM4BOD_HYST}		—	46	—	mV
EM4 response time	t_{EM4BOD_DELAY}	Supply drops at 0.1V/µs rate	—	300	—	µs

4.1.7 Frequency Synthesizer Characteristics

Table 4.10. Frequency Synthesizer Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF Synthesizer Frequency range	F_{RANGE_2400}	2.4 GHz frequency range	2400	—	2483.5	MHz
LO tuning frequency resolution with 38.4 MHz crystal	F_{RES_2400}	2400 - 2483.5 MHz	—	—	73	Hz
Maximum frequency deviation with 38.4 MHz crystal	ΔF_{MAX_2400}		—	—	1677	kHz

4.1.8 2.4 GHz RF Transceiver Characteristics

4.1.8.1 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_{OP} = 25 °C,VDD = 3.3 V, DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.11. RF Transmitter General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum TX power +8dBm rated parts	$POUT_{MAX}$		—	+8	—	dBm
Maximum TX power +2dBm rated parts	$POUT_{MAX}$		—	+2	—	dBm
Minimum active TX Power	$POUT_{MIN}$	CW		-26	—	dBm
Output power step size	$POUT_{STEP}$	-5 dBm < Output power < 0 dBm	—	1	—	dB
		0 dBm < output power < $POUT_{MAX}$	—	0.5	—	dB
Output power variation vs supply at $POUT_{MAX}$	$POUT_{VAR\_V}$	2.4 V < $V_{VREGVDD}$ < 3.3 V using DC-DC converter	—	2.2	—	dB
Output power variation vs temperature at $POUT_{MAX}$	$POUT_{VAR\_T}$	From -40 to +85 °C, PAVDD connected to DC-DC output	—	1.5	—	dB
Output power variation vs RF frequency at $POUT_{MAX}$	$POUT_{VAR\_F}$	Over RF tuning frequency range	—	0.4	—	dB
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz

4.1.8.2 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_{OP} = 25 °C,VDD = 3.3 V, DC-DC on. Crystal frequency =38.4 MHz. RF center frequency 2.440 GHz. Conducted measurement from the antenna feedpoint.

Table 4.12. RF Receiver General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Receive mode maximum spurious emission	$SPUR_{RX}$	30 MHz to 1 GHz	—	-57	—	dBm
		1 GHz to 12 GHz	—	-47	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$SPUR_{RX\_FCC}$	216 MHz to 960 MHz, Conducted Measurement	—	-55.2	—	dBm
		Above 960 MHz, Conducted Measurement	—	-47.2	—	dBm

4.1.8.3 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_{OP} = 25 °C,VDD = 3.3 V. Crystal frequency = 38.4 MHz. RF center frequency 2.440 GHz. DC-DC on. Conducted measurement from the antenna feedpoint.

Table 4.13. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 0.1% BER	SAT	Signal is reference signal[1]. Packet length is 20 bytes.	—	10	—	dBm
30.8% Packet Error Rate[2]	SENS	With non-ideal signals as specified in RF-PHY.TS.4.2.2, section 4.6.1	—	-90	—	dBm
Signal to co-channel interferer, 0.1% BER	C/I_{CC}	Desired signal 3 dB above reference sensitivity	—	8.3	—	dB
Blocking, 0.1% BER, Desired is reference signal at -67 dBm. Interferer is CW in OOB range.	$BLOCK_{OOB}$	Interferer frequency 30 MHz ≤ f ≤ 2000 MHz	—	-27	—	dBm
		Interferer frequency 2003 MHz ≤ f ≤ 2399 MHz	—	-32	—	dBm
		Interferer frequency 2484 MHz ≤ f ≤ 2997 MHz	—	-32	—	dBm
		Interferer frequency 3 GHz ≤ f ≤ 12.75 GHz	—	-27	—	dBm
Intermodulation performance	IM	Per Core_4.1, Vol 6, Part A, Section 4.4 with n = 3	—	-25.8	—	dBm
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		—	—	5	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		-98	—	—	dBm
RSSI resolution	$RSSI_{RES}$	Over $RSSI_{MIN}$ to $RSSI_{MAX}$	—	—	0.5	dB

Note:

1. Reference signal is defined 2GFSK at -67 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 1 Mbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm
2. Receive sensitivity on Bluetooth Low Energy channel 26 is -86 dBm

4.1.9 Oscillators

4.1.9.1 LFXO

Table 4.14. LFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		—	32.768	—	kHz
Overall frequency tolerance in all conditions[1]			-100		100	ppm

Note:
1. XTAL nominal frequency tolerance = +/- 20 ppm

4.1.9.2 HFXO

Table 4.15. HFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXO}		-	38.4	-	MHz
Crystal frequency tolerance			-40		40	ppm

4.1.9.3 LFRCO

Table 4.16. LFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	30.474	32.768	34.243	kHz
		ENVREF = 0 in CMU_LFRCOCTRL	30.474	32.768	33.915	kHz
Startup time	t_{LFRCO}		—	500	—	µs
Current consumption [1]	I_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	—	342	—	nA
		ENVREF = 0 in CMU_LFRCOCTRL	—	494	—	nA

Note:
1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register

4.1.9.4 HFRCO and AUXHFRCO

Table 4.17. HFRCO and AUXHFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Accuracy	f_{HFRCO}	Any frequency band, across supply voltage and temperature	-2.5	—	2.5	%
Start-up time	t_{HFRCO}	f_{HFRCO} ≥ 19 MHz	—	300	—	ns
		4 < f_{HFRCO} < 19 MHz	—	1	—	µs
		f_{HFRCO} ≤ 4 MHz	—	2.5	—	µs
Current consumption on all supplies	I_{HFRCO}	f_{HFRCO} = 38 MHz	—	204	228	µA
		f_{HFRCO} = 32 MHz	—	171	190	µA
		f_{HFRCO} = 26 MHz	—	147	164	µA
		f_{HFRCO} = 19 MHz	—	126	138	µA
		f_{HFRCO} = 16 MHz	—	110	120	µA
		f_{HFRCO} = 13 MHz	—	100	110	µA
		f_{HFRCO} = 7 MHz	—	81	91	µA
		f_{HFRCO} = 4 MHz	—	33	35	µA
		f_{HFRCO} = 2 MHz	—	31	35	µA
		f_{HFRCO} = 1 MHz	—	30	35	µA
Step size	SS_{HFRCO}	Coarse (% of period)	—	0.8	—	%
		Fine (% of period)	—	0.1	—	%
Period Jitter	PJ_{HFRCO}		—	0.2	—	% RMS

4.1.9.5 ULFRCO

Table 4.18. ULFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}		0.95	1	1.07	kHz

4.1.10 Flash Memory Characteristics

Table 4.19. Flash Memory Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		10000	—	—	cycles
Flash data retention	RET_{FLASH}		10	—	—	years
Word (32-bit) programming time	t_{W_PROG}		20	26	40	µs
Page erase time	t_{PERASE}		20	27	40	ms
Mass erase time	t_{MERASE}		20	27	40	ms
Device erase time[2]	t_{DERASE}		—	60	74	ms
Page erase current[3]	I_{ERASE}		—	—	3	mA
Mass or Device erase current[3]			—	—	5	mA
Write current[3]	I_{WRITE}		—	—	3	mA

Note:

1. Flash data retention information is published in the Quarterly Quality and Reliability Report.
2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW)
3. Measured at 25°C

4.1.11 GPIO

For the table below, see Figure 3.2 Power Supply Configuration on page 9 on page 5 to see the relation between the modules external VDD pin and internal voltage supplies. The module itself has only one external power supply input (VDD).

Table 4.20. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IOIL}	GPIO pins	—	—	IOVDD*0.3	V
		RESETn	—	—	AVDD*0.3	V
Input high voltage	V_{IOIH}	GPIO pins	IOVDD*0.7	—	—	V
		RESETn	AVDD*0.7	—	—	V
Output high voltage relative to IOVDD	V_{IOOH}	Sourcing 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.8	—	—	V
		Sourcing 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.6	—	—	V
		Sourcing 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.8	—	—	V
		Sourcing 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.6	—	—	V
Output low voltage relative to IOVDD	V_{IOOL}	Sinking 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.2	V
		Sinking 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.4	V
		Sinking 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.2	V
		Sinking 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.4	V
Input leakage current	I_{IOLEAK}	All GPIO except LFXO pins, GPIO ≤ IOVDD	—	0.1	30	nA
		LFXO Pins, GPIO ≤ IOVDD	—	0.1	50	nA
Input leakage current on 5VTOL pads above IOVDD	$I_{5VTOLLEAK}$	IOVDD < GPIO ≤ IOVDD + 2 V	—	3.3	15	µA
I/O pin pull-up resistor	R_{PU}		30	43	65	kΩ
I/O pin pull-down resistor	R_{PD}		30	43	65	kΩ
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		20	25	35	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output fall time, From 70% to 30% of V_{IO}	t_{IOOF}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE[1] = 0x6	—	1.8	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	4.5	—	ns
Output rise time, From 30% to 70% of V_{IO}	t_{IOOR}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE = 0x6[1]	—	2.2	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	7.4	—	ns
RESETn low time to ensure pin reset	T_{RESET}		100	—	—	ns

Note:
1. In GPIO_Pn_CTRL register

4.1.12 VMON

Table 4.21. VMON

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VMON Supply Current	I_{VMON}	In EM0 or EM1, 1 supply monitored	—	5.8	8.26	µA
		In EM0 or EM1, 4 supplies monitored	—	11.8	16.8	µA
		In EM2, EM3 or EM4, 1 supply monitored	—	62	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored	—	99	—	nA
VMON Loading of Monitored Supply	I_{SENSE}	In EM0 or EM1	—	2	—	µA
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	V_{VMON_RANGE}		1.62	—	3.4	V
Threshold step size	N_{VMON_STESP}	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	t_{VMON_RES}	Supply drops at 1V/µs rate	—	460	—	ns
Hysteresis	V_{VMON_HYST}		—	26	—	mV

4.1.13 ADC

For the table below, see Figure 3.2 Power Supply Configuration on page 9 to see the relation between the modules external VDD pin and internal voltage supplies. The module itself has only one external power supply input (VDD).

Table 4.22. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	$V_{RESOLUTION}$		6	—	12	Bits
Input voltage range	V_{ADCIN}	Single ended	0	—	$2*V_{REF}$	V
		Differential	$-V_{REF}$	—	V_{REF}	V
Input range of external reference voltage, single ended and differential	$V_{ADCREFIN\_P}$		1	—	V_{AVDD}	V
Power supply rejection[1]	$PSRR_{ADC}$	At DC	—	80	—	dB
Analog input common mode rejection ratio	$CMRR_{ADC}$	At DC	—	80	—	dB
Current from all supplies, using internal reference buffer. Continous operation. WARMUPMODE[2] = KEEPADCWARM	$I_{ADC\_CONTINOUS\_LP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	301	350	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 [3]	—	149	—	µA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 [3]	—	91	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[2] = NORMAL	$I_{ADC\_NORMAL\_LP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	51	—	µA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 [3]	—	9	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[2] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_LP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	117	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	79	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current from all supplies, using internal reference buffer. Continous operation. WARMUPMODE[2] = KEEPADCWARM	$I_{ADC\_CONTINOUS\_HP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	345	—	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 [3]	—	191	—	µA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 [3]	—	132	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[2] = NORMAL	$I_{ADC\_NORMAL\_HP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	102	—	µA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 [3]	—	17	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[2] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_HP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	162	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	123	—	µA
Current from HFPERCLK	I_{ADC_CLK}	HFPERCLK = 16 MHz	—	140	—	µA
ADC Clock Frequency	f_{ADCCLK}		—	—	16	MHz
Throughput rate	$f_{ADCRATE}$		—	—	1	Msps
Conversion time[4]	$t_{ADCCONV}$	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core	$t_{ADCSTART}$	WARMUPMODE[2] = NORMAL	—	—	5	µs
		WARMUPMODE[2] = KEEPINSTANDBY	—	—	2	µs
		WARMUPMODE[2] = KEEPINSLOWACC	—	—	1	µs
SNDR at 1Msps and f_{in} = 10kHz	$SNDR_{ADC}$	Internal reference, 2.5 V full-scale, differential (-1.25, 1.25)	58	67	—	dB
		vrefp_in = 1.25 V direct mode with 2.5 V full-scale, differential	—	68	—	dB
Spurious-Free Dynamic Range (SFDR)	$SFDR_{ADC}$	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Input referred ADC noise, rms	V_{REF_NOISE}	Including quantization noise and distortion	—	380	—	µV
Offset Error	$V_{ADCOFFSETERR}$		-3	0.25	3	LSB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Gain error in ADC	V_{ADC_GAIN}	Using internal reference	—	-0.2	3.5	%
		Using external reference	—	-1	—	%
Differential non-linearity (DNL)	DNL_{ADC}	12 bit resolution	-1	—	2	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	12 bit resolution	-6	—	6	LSB
Temperature Sensor Slope	V_{TS_SLOPE}		—	-1.84	—	mV/°C

Note:

1. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL
2. In ADCn_CNTL register
3. In ADCn_BIASPROG register
4. Derived from ADCCLK

4.1.14 IDAC

For the table below, see Figure 3.2 Power Supply Configuration on page 9 on page 5 to see the relation between the modules external VDD pin and internal voltage supplies. The module itself has only one external power supply input (VDD).

Table 4.23. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Number of Ranges	N_{IDAC_RANGES}		—	4	—	-
Output Current	I_{IDAC_OUT}	RANGSEL[1] = RANGE0	0.05	—	1.6	µA
		RANGSEL[1] = RANGE1	1.6	—	4.7	µA
		RANGSEL[1] = RANGE2	0.5	—	16	µA
		RANGSEL[1] = RANGE3	2	—	64	µA
Linear steps within each range	N_{IDAC_STEPS}		—	32	—	
Step size	SS_{IDAC}	RANGSEL[1] = RANGE0	—	50	—	nA
		RANGSEL[1] = RANGE1	—	100	—	nA
		RANGSEL[1] = RANGE2	—	500	—	nA
		RANGSEL[1] = RANGE3	—	2	—	µA
Total Accuracy, STEPSEL[1] = 0x10	ACC_{IDAC}	EM0 or EM1, AVDD=3.3 V, T = 25 °C	-2	—	2	%
		EM0 or EM1	-18	—	22	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C	—	-2	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C	—	-1.7	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.8	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C	—	-0.7	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C	—	-0.6	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Start up time	t_{IDAC_SU}	Output within 1% of steady state value	—	5	—	µs
Settling time, (output settled within 1% of steady state value)	t_{IDAC_SETTLE}	Range setting is changed	—	5	—	µs
		Step value is changed	—	1	—	µs
Current consumption in EM0 or EM1 [2]	I_{IDAC}	Source mode, excluding output current	—	8.9	13	µA
		Sink mode, excluding output current	—	12	16	µA
Current consumption in EM2 or EM3[2]		Source mode, excluding output current, duty cycle mode, T = 25 °C	—	1.04	—	µA
		Sink mode, excluding output current, duty cycle mode, T = 25 °C	—	1.08	—	µA
		Source mode, excluding output current, duty cycle mode, T ≥ 85 °C	—	8.9	—	µA
		Sink mode, excluding output current, duty cycle mode, T ≥ 85 °C	—	12	—	µA
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	I_{COMP_SRC}	RANGESEL1=0, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mv)	—	0.04	—	%
		RANGESEL1=1, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mV)	—	0.02	—	%
		RANGESEL1=2, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-150 mV)	—	0.02	—	%
		RANGESEL1=3, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-250 mV)	—	0.02	—	%
Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD	I_{COMP_SINK}	RANGESEL1=0, output voltage = 100 mV	—	0.18	—	%
		RANGESEL1=1, output voltage = 100 mV	—	0.12	—	%
		RANGESEL1=2, output voltage = 150 mV	—	0.08	—	%
		RANGESEL1=3, output voltage = 250 mV	—	0.02	—	%

Note:

1. In IDAC_CURPROG register
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.15 Analog Comparator (ACMP)

Table 4.24. ACMP

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ACMPIN}	ACMPVDD = ACMPn_CTRL_PWRSEL [1]	0	—	$V_{ACMPVDD}$	V
Supply Voltage	$V_{ACMPVDD}$	BIASPROG[2] ≤ 0x10 or FULLBIAS[2] = 0	1.85	—	$V_{VREGVDD\_MAX}$	V
		0x10 < BIASPROG[2] ≤ 0x20 and FULLBIAS[2] = 1	2.1	—	$V_{VREGVDD\_MAX}$	V
Active current not including voltage reference	I_{ACMP}	BIASPROG[2] = 0x10, FULLBIAS[2] = 0	—	306	—	nA
		BIASPROG[2] = 0x20, FULLBIAS[2] = 1	—	74	95	µA
Current consumption of internal voltage reference	$I_{ACMPREF}$	VLP selected as input using 2.5 V Reference / 4 (0.625 V)	—	50	—	nA
		VLP selected as input using VDD	—	20	—	nA
		VBDIV selected as input using 1.25 V reference / 1	—	4.1	—	µA
		VADIV selected as input using VDD/1	—	2.4	—	µA
Hysteresis (V_{CM} = 1.25 V, BIASPROG[2] = 0x10, FULLBIAS[2] = 1)	$V_{ACMPHYST}$	HYSTSEL[3] = HYST0	-1.75	0	1.75	mV
		HYSTSEL[3] = HYST1	10	18	26	mV
		HYSTSEL[3] = HYST2	21	32	46	mV
		HYSTSEL[3] = HYST3	27	44	63	mV
		HYSTSEL[3] = HYST4	32	55	80	mV
		HYSTSEL[3] = HYST5	38	65	100	mV
		HYSTSEL[3] = HYST6	43	77	121	mV
		HYSTSEL[3] = HYST7	47	86	148	mV
		HYSTSEL[3] = HYST8	-4	0	4	mV
		HYSTSEL[3] = HYST9	-27	-18	-10	mV
		HYSTSEL[3] = HYST10	-47	-32	-18	mV
		HYSTSEL[3] = HYST11	-64	-43	-27	mV
		HYSTSEL[3] = HYST12	-78	-54	-32	mV
		HYSTSEL[3] = HYST13	-93	-64	-37	mV
		HYSTSEL[3] = HYST14	-113	-74	-42	mV
		HYSTSEL[3] = HYST15	-135	-85	-47	mV

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Comparator delay[4]	$t_{ACMPDELAY}$	BIASPROG[2] = 0x10, FULLBIAS[2] = 0	—	3.7	—	µs
		BIASPROG[2] = 0x20, FULLBIAS[2] = 1	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	BIASPROG[2] =0x10, FULLBIAS[2] = 1	-35	—	35	mV
Reference Voltage	$V_{ACMPREF}$	Internal 1.25 V reference	1	1.25	1.47	V
		Internal 2.5 V reference	2	2.5	2.8	V
Capacitive Sense Internal Resistance	R_{CSRES}	CSRESSEL[5] = 0	—	inf	—	kΩ
		CSRESSEL[5] = 1	—	15	—	kΩ
		CSRESSEL[5] = 2	—	27	—	kΩ
		CSRESSEL[5] = 3	—	39	—	kΩ
		CSRESSEL[5] = 4	—	51	—	kΩ
		CSRESSEL[5] = 5	—	102	—	kΩ
		CSRESSEL[5] = 6	—	164	—	kΩ
		CSRESSEL[5] = 7	—	239	—	kΩ

Note:

1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD
2. In ACMPn_CTRL register
3. In ACMPn_HYSTERESIS register
4. ±100 mV differential drive
5. In ACMPn_INPUTSEL register

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given as:

$$\mathbf{I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}}$$

$\mathbf{I_{ACMPREF}}$ is zero if an external voltage reference is used.

4.1.16 I2C

I2C Standard-mode (Sm)

Table 4.25. I2C Standard-mode (Sm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	µs
SCL clock high time	t_{HIGH}		4	—	—	µs
SDA set-up time	$t_{SU,DAT}$		250	—	—	ns
SDA hold time[3]	$t_{HD,DAT}$		100	—	3450	ns
Repeated START condition set-up time	$t_{SU,STA}$		4.7	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$		4	—	—	µs
STOP condition set-up time	$t_{SU,STO}$		4	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	µs

Note:

1. For CLHR set to 0 in the I2Cn_CTRL register
2. For the minimum HFPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW})

I2C Fast-mode (Fm)

Table 4.26. I2C Fast-mode (Fm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time	t_{HIGH}		0.6	—	—	µs
SDA set-up time	$t_{SU,DAT}$		100	—	—	ns
SDA hold time[3]	$t_{HD,DAT}$		100	—	900	ns
Repeated START condition set-up time	$t_{SU,STA}$		0.6	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$		0.6	—	—	µs
STOP condition set-up time	$t_{SU,STO}$		0.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	µs

Note:

1. For CLHR set to 1 in the I2Cn_CTRL register
2. For the minimum HFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW})

I2C Fast-mode Plus (Fm+)

Table 4.27. I2C Fast-mode Plus (Fm+)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	µs
SCL clock high time	t_{HIGH}		0.26	—	—	µs
SDA set-up time	$t_{SU,DAT}$		50	—	—	ns
SDA hold time	$t_{HD,DAT}$		100	—	—	ns
Repeated START condition set-up time	$t_{SU,STA}$		0.26	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$		0.26	—	—	µs
STOP condition set-up time	$t_{SU,STO}$		0.26	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	µs

Note:
1. For CLHR set to 0 or 1 in the I2Cn_CTRL register
2. For the minimum HFPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual

4.1.17 USART SPI

SPI Master Timing

Table 4.28. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [2]	t_{SCLK}		2 * $t_{HFPERCLK}$	—	—	ns
CS to MOSI [1] [2]	t_{CS_MO}		0	—	8	ns
SCLK to MOSI [1] [2]	t_{SCLK_MO}		3	—	20	ns
MISO setup time [1] [2]	t_{SU_MI}	IOVDD = 1.62 V	56	—	—	ns
		IOVDD = 3.0 V	37	—	—	ns
MISO hold time [1] [2]	t_{H_MI}		6	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

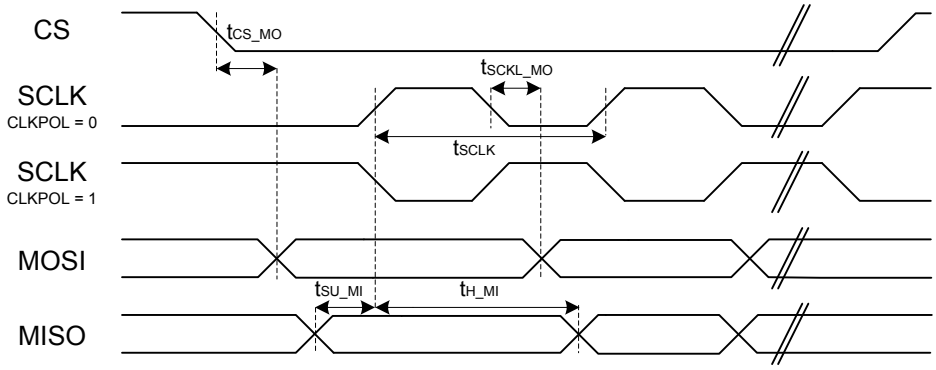


Figure 4.1. SPI Master Timing Diagram (SMSDELAY = 0)

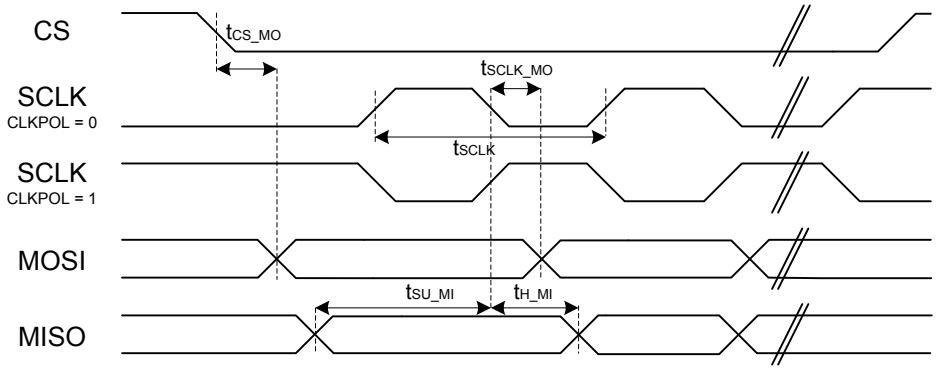


Figure 4.2. SPI Master Timing Diagram (SMSDELAY = 1)

SPI Slave Timing

Table 4.29. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCKL period [1] [2]	t_{SCLK_sl}		2 * $t_{HFPERCLK}$	—	—	ns
SCLK high period[1] [2]	t_{SCLK_hi}		3 * $t_{HFPERCLK}$	—	—	ns
SCLK low period [1,2]	t_{SCLK_lo}		3 * $t_{HFPERCLK}$	—	—	ns
CS active to MISO [1] [2]	$t_{CS\_ACT\_MI}$		4	—	50	ns
CS disable to MISO [1] [2]	$t_{CS\_DIS\_MI}$		4	—	50	ns
MOSI setup time [1] [2]	t_{SU_MO}		4	—	—	ns
MOSI hold time [1] [2]	t_{H_MO}		3 + 2 * $t_{HFPERCLK}$	—	—	ns
SCLK to MISO [1] [2]	t_{SCLK_MI}		16 + $t_{HFPERCLK}$	—	66 + 2 * $t_{HFPERCLK}$	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

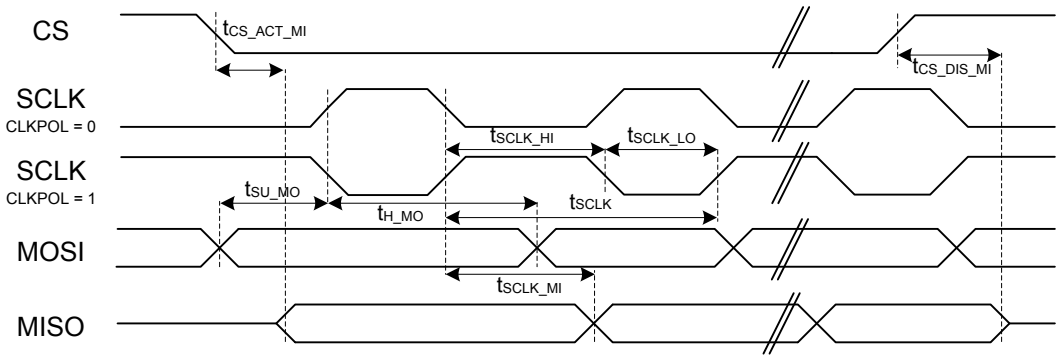


Figure 4.3. SPI Slave Timing Diagram

5. Typical Connection Diagrams

5.1 Typical Connections

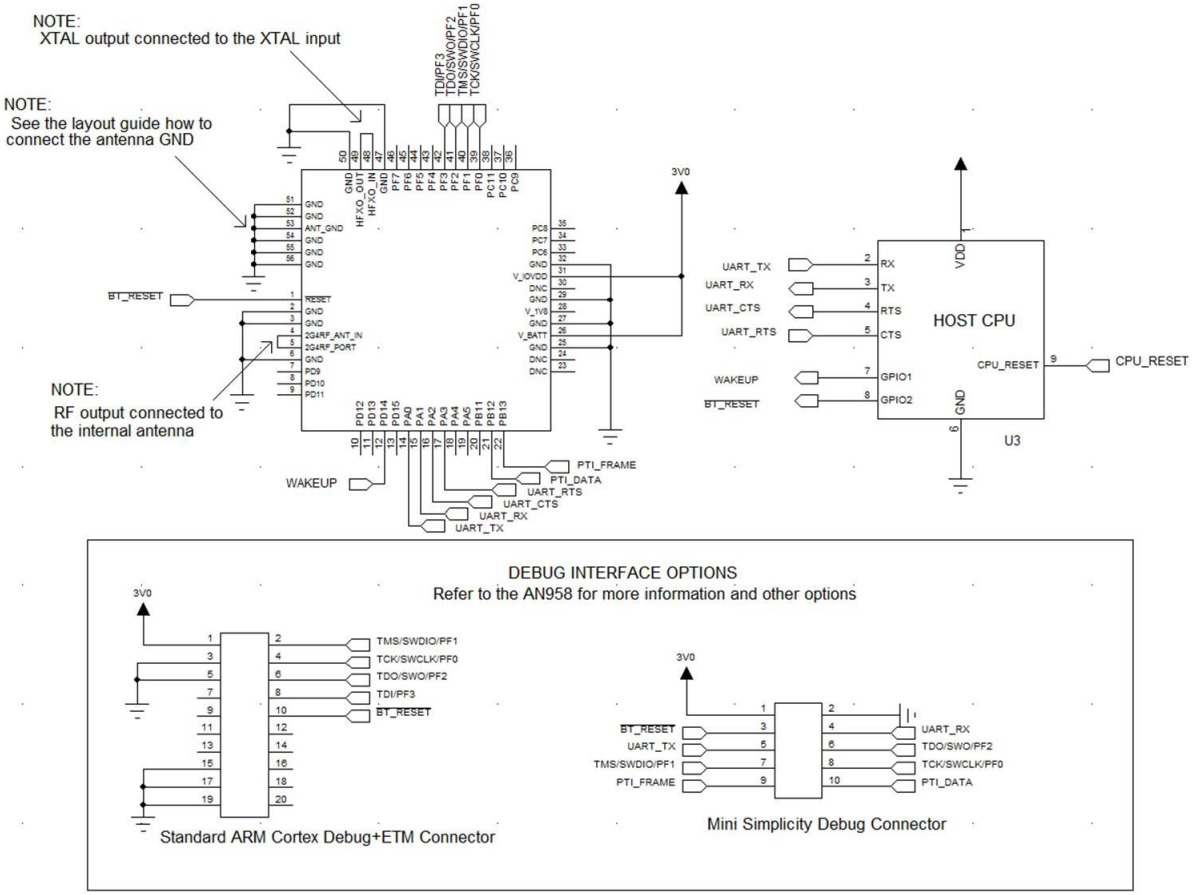
The figure below shows a typical reference schematic and how to connect:

- Power supplies and Ground pins
- Antenna loop for internal antenna usage
- XTAL loop
- Debug port
- Reset line
- Optional UART connection to an external host for Network Co-Processor (NCP) usage

Note: It's recommended to connect the reset line to the host CPU when NCP mode is used.

Note: The V_1V8 pin is the 1.8V output of the internal DC-DC converter. This pin should be left unconnected. Do not add external decoupling or power external circuits from this pin.

Figure 5.1. Typical Connections



6. Layout Guidelines

For optimal performance of the BGM11S, please follow the PCB layout guidelines and ground plane recommendations indicated in this section.

6.1 Layout Guidelines

This section contains generic PCB layout and design guidelines for the BGM11S module. Generally, please follow these guidelines:

- Place the module at the edge of the PCB, as shown in the figures in this chapter.
- Do not place any metal (traces, components, etc.) in the antenna clearance area.
- Connect all ground pads directly to a solid ground plane.
- Place the ground vias as close to the ground pads as possible.

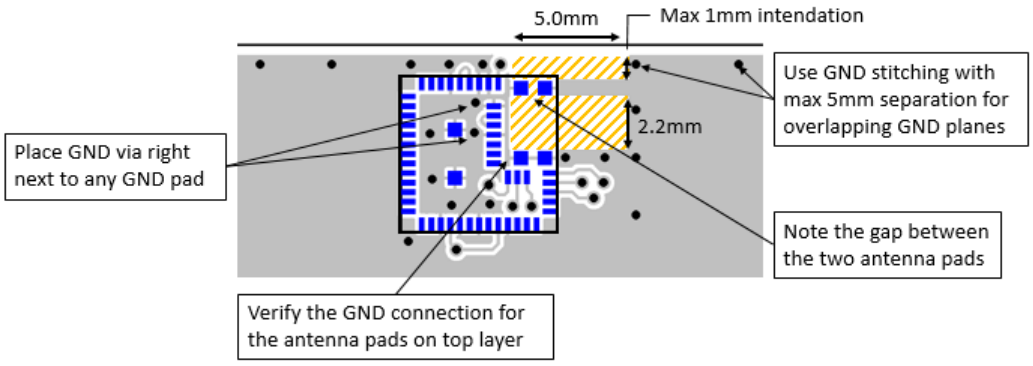


Figure 6.1. BGM11S PCB Top Layer Design

Following rules are recommended for the PCB design:

- Trace to copper clearance 150 µm
- PTH drill size 300 µm
- PTH annular ring 150 µm

Important:

The antenna area must align with the pads precisely. Please refer to the recommended PCB land pattern for exact dimensions.

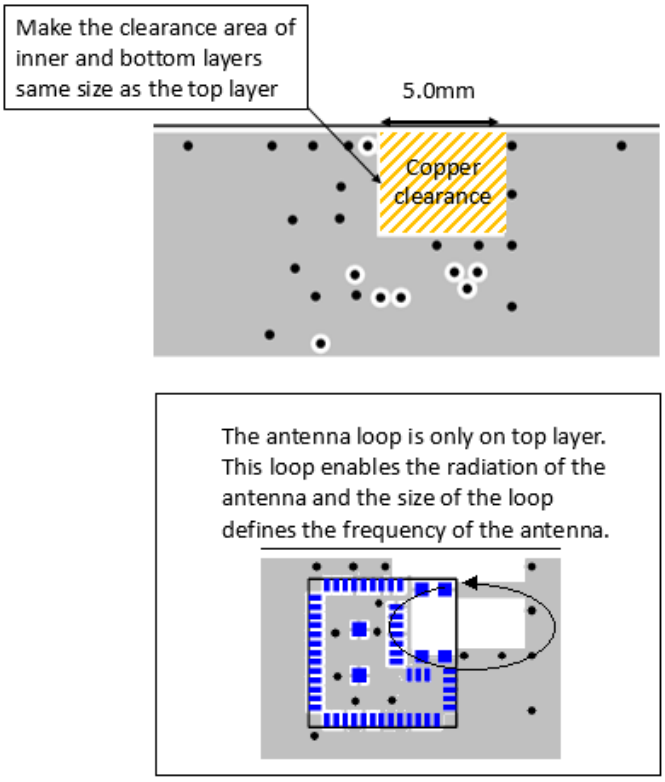


Figure 6.2. BGM11S PCB Middle and Bottom Layer Design

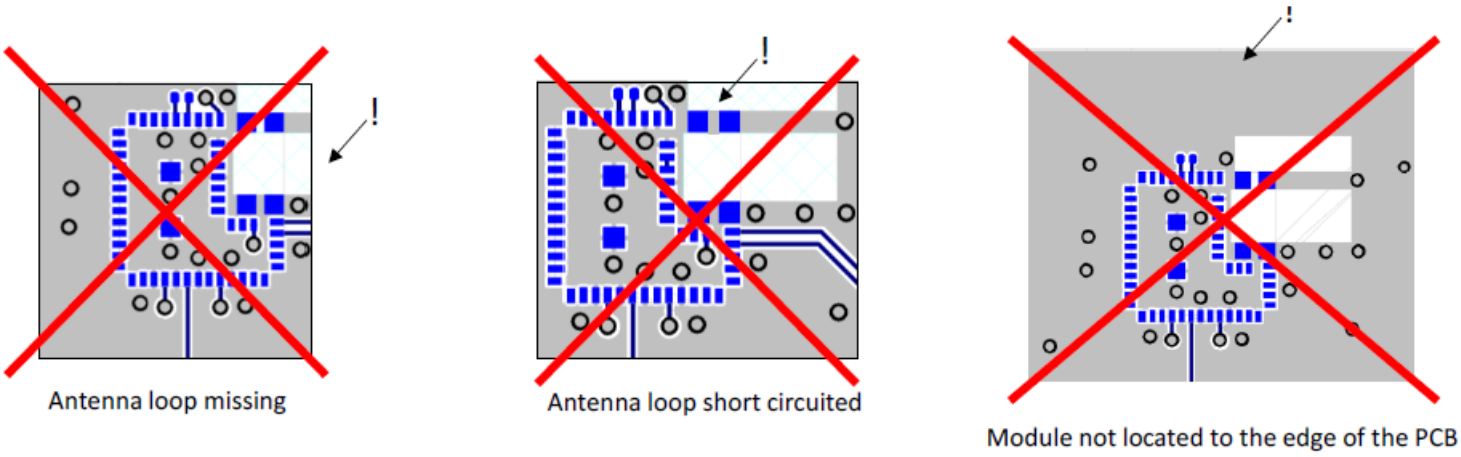


Figure 6.3. Poor Layout Designs for the BGM11S

Layout checklist for BGM11S:

1. Antenna area is aligned relative to the module pads as shown in the recommended PCB land pattern
2. Clearance area within the inner layers and bottom layer is covering the whole antenna area as shown in the layoyt guidelines
3. The antenna loop is implemented on top layer as shown in the layoyt guidelines
4. All dimensions within the antenna area are precisely as shown in the recommended PCB land pattern
5. The module is placed to the edge of the PCB with max 1mm intendation
6. The mdoule is not placed to the corner of the PCB

6.2 Effect of PCB Width

The BGM11S module should be placed at the center of the PCB edge because the width of the board has an impact to the radiated efficiency but more importantly there should be enough ground plane on both sides of the module for optimal antenna performance. The figure below gives an indcation of ground plane size vs. maximum achievable range.

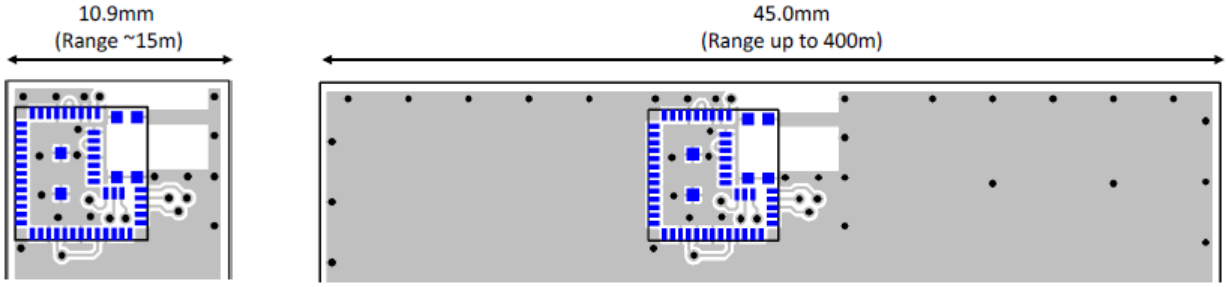


Figure 6.4. BGM11S PCB Top Layer Design

The impact of the board size to the radiated performance is a generic feature of all PCB and chip antennas and it is not a unique feature of BGM11S. In case of BGM11S the depth of the board is not important and it doesn't impact the radiated performance.

6.3 Effect of Plastic and Metal Materials

The antenna on the BGM11S. is insensitive to the effects of nearby plastic and other materials with low dielectric constant and no separation between the BGM11S. and plastic or other materials is needed. Also the board thickness doesn't have any impact the module.

Any metal within the antenna area or in close proximity to the antenna area may detune the antenna. In this case it is possible to retune the antenna by adjusting the width of the antenna loop. To avoid detuning of the antenna the minimum distance to any metal should be more than 3mm. Encapsulating the module inside metal casing will prevent the radiation of the antenna.

Following picture shows how it is possible to adjust the frequency of the antenna. The antenna is extremely robust against any objects in close proximity or in direct touch with the antenna and it is recommended not to adjust the dimensions of the antenna area unless it is clear that a metal object, such as a coin cell battery, within the antenna area is detuning the antenna.

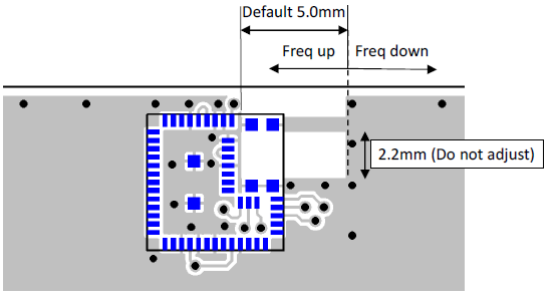


Figure 6.5. Tuning the Antenna by Adjusting the Width of the Antenna Loop

6.4 Effect of Human Body

Placing the module in touch or very close to the human body will negatively impact antenna efficiency and reduce range.

6.5 2D Radiation Pattern Plots

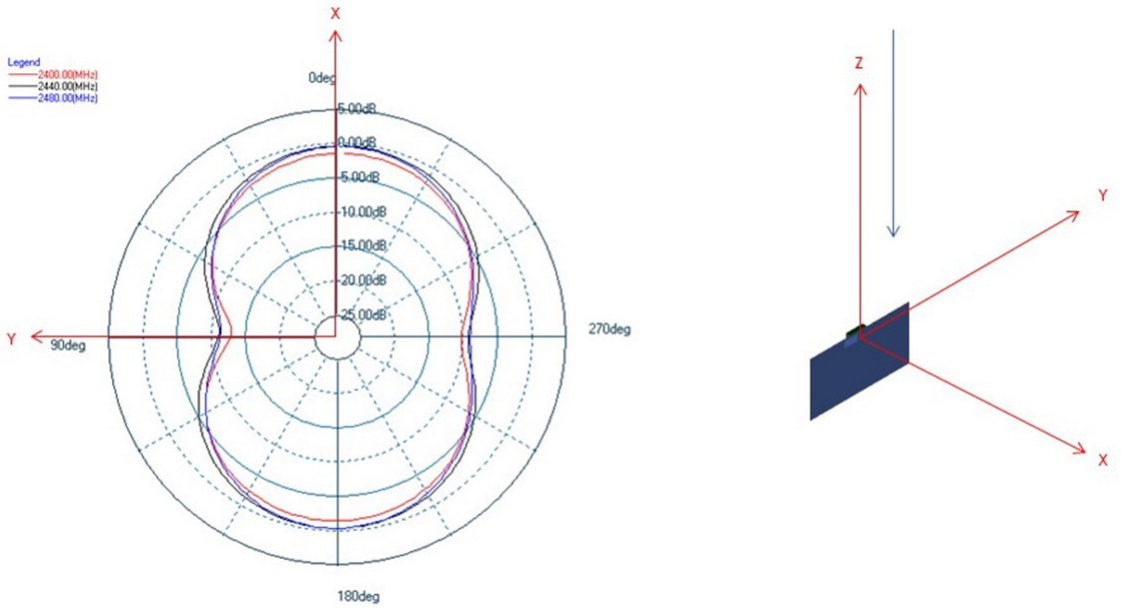


Figure 6.6. Typical 2D Radiation Pattern – Front View

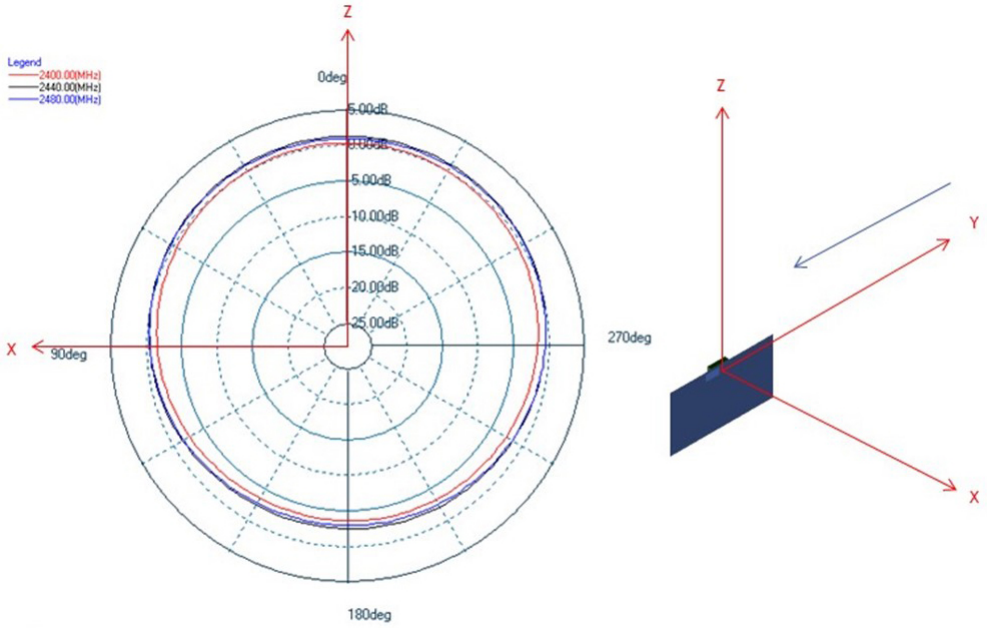


Figure 6.7. Typical 2D Radiation Pattern – Side View

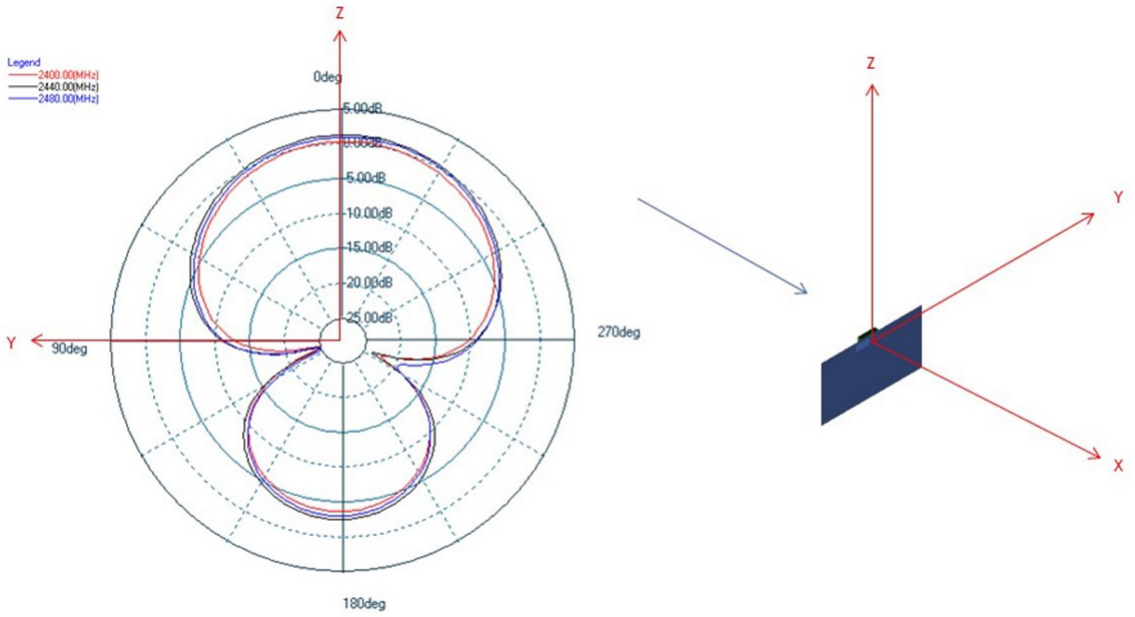


Figure 6.8. Typical 2D Radiation Pattern – Top View

7. Pin Definitions

7.1 Pin Definitions

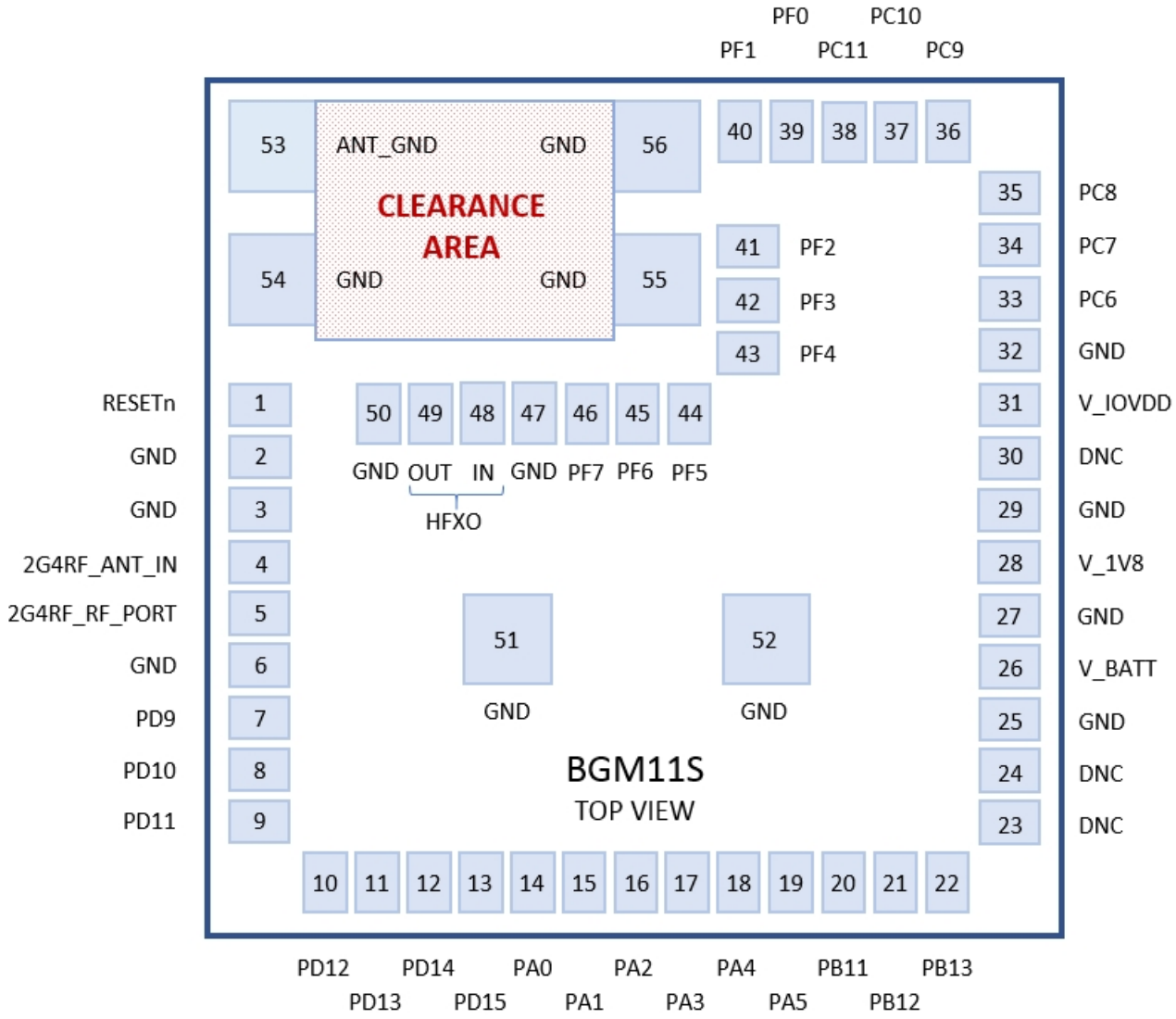


Figure 7.1. BGM11S Pinout

Table 7.1. Device Pinout

		Pin Alternate Functionality / Description				
Pin #	**Pin Name**	**Analog**	**Timers**	**Communication**	**Radio**	**Other**
1	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
2	GND	Ground				
3	GND	Ground				
4	2G4RF_ANT_IN	50 ohm input pin for the internal 2.4GHz antenna				
5	2G4RF_RF_PORT	50 ohm 2.4GHz RF input and output				
6	GND	Ground				
23	DNC	Do not connect but leave floating				
24	DNC	Do not connect but leave floating				
25	GND	Ground				
26	V_BATT	1.85 - 3.8VDC input to the internal DC-DC converter and AVDD. Internally decoupled and does not require decoupling capacitors.				
27	GND	Ground				
28	V_1V8	1.8V output of the internal DC-DC converter. Internally decoupled so do not use an external decoupling capacitor.				
29	GND	Ground				
30	DNC	Do not connect but leave floating				
31	V_IOVDD	Digital I/O power supply.				
32	GND	Ground				
47	GND	Ground				
48	HFXO_IN	38.4MHz XTAL input. Connect to HFXO_OUT.				
49	HFXO_OUT	38.4MHz XTAL output. Connect to HFXO_IN.				
50	GND	Ground				
51	GND	Ground				
52	GND	Ground				
53	ANT_GND	Antenna ground				
54	GND	Ground				
55	GND	Ground				
56	GND	Ground				

		Pin Alternate Functionality / Description				
Pin #	**Pin Name**	**Analog**	**Timers**	**Communication**	**Radio**	**Other**
7	PD9	BUSCY [ADC0: APORT3YCH1 ACMP0: APORT3YCH1 ACMP1: APORT3YCH1 IDAC0: APORT1YCH1] BUSDX [ADC0: APORT4XCH1 ACMP0: APORT4XCH1 ACMP1: APORT4XCH1]	TIM0_CC0 #17 TIM0_CC1 #16 TIM0_CC2 #15 TIM0_CDTI0 #14 TIM0_CDTI1 #13 TIM0_CDTI2 #12 TIM1_CC0 #17 TIM1_CC1 #16 TIM1_CC2 #15 TIM1_CC3 #14 LE-TIM0_OUT0 #17 LETIM0_OUT1 #16 PCNT0_S0IN #17 PCNT0_S1IN #16	US0_TX #17 US0_RX #16 US0_CLK #15 US0_CS #14 US0_CTS #13 US0_RTS #12 US1_TX #17 US1_RX #16 US1_CLK #15 US1_CS #14 US1_CTS #13 US1_RTS #12 LEU0_TX #17 LEU0_RX #16 I2C0_SDA #17 I2C0_SCL #16	FRC_DCLK #17 FRC_DOUT #16 FRC_DFRAME #15 MODEM_DCLK #17 MODEM_DIN #16 MO-DEM_DOUT #15 MODEM_ANT0 #14 MO-DEM_ANT1 #13	CMU_CLK0 #4 PRS_CH3 #8 PRS_CH4 #0 PRS_CH5 #6 PRS_CH6 #11 ACMP0_O #17 ACMP1_O #17
8	PD10	BUSCX [ADC0: APORT3XCH2 ACMP0: APORT3XCH2 ACMP1: APORT3XCH2 IDAC0: APORT1XCH2] BUSDY [ADC0: APORT4YCH2 ACMP0: APORT4YCH2 ACMP1: APORT4YCH2]	TIM0_CC0 #18 TIM0_CC1 #17 TIM0_CC2 #16 TIM0_CDTI0 #15 TIM0_CDTI1 #14 TIM0_CDTI2 #13 TIM1_CC0 #18 TIM1_CC1 #17 TIM1_CC2 #16 TIM1_CC3 #15 LE-TIM0_OUT0 #18 LETIM0_OUT1 #17 PCNT0_S0IN #18 PCNT0_S1IN #17	US0_TX #18 US0_RX #17 US0_CLK #16 US0_CS #15 US0_CTS #14 US0_RTS #13 US1_TX #18 US1_RX #17 US1_CLK #16 US1_CS #15 US1_CTS #14 US1_RTS #13 LEU0_TX #18 LEU0_RX #17 I2C0_SDA #18 I2C0_SCL #17	FRC_DCLK #18 FRC_DOUT #17 FRC_DFRAME #16 MODEM_DCLK #18 MODEM_DIN #17 MO-DEM_DOUT #16 MODEM_ANT0 #15 MO-DEM_ANT1 #14	CMU_CLK1 #4 PRS_CH3 #9 PRS_CH4 #1 PRS_CH5 #0 PRS_CH6 #12 ACMP0_O #18 ACMP1_O #18
9	PD11	BUSCY [ADC0: APORT3YCH3 ACMP0: APORT3YCH3 ACMP1: APORT3YCH3 IDAC0: APORT1YCH3] BUSDX [ADC0: APORT4XCH3 ACMP0: APORT4XCH3 ACMP1: APORT4XCH3]	TIM0_CC0 #19 TIM0_CC1 #18 TIM0_CC2 #17 TIM0_CDTI0 #16 TIM0_CDTI1 #15 TIM0_CDTI2 #14 TIM1_CC0 #19 TIM1_CC1 #18 TIM1_CC2 #17 TIM1_CC3 #16 LE-TIM0_OUT0 #19 LETIM0_OUT1 #18 PCNT0_S0IN #19 PCNT0_S1IN #18	US0_TX #19 US0_RX #18 US0_CLK #17 US0_CS #16 US0_CTS #15 US0_RTS #14 US1_TX #19 US1_RX #18 US1_CLK #17 US1_CS #16 US1_CTS #15 US1_RTS #14 LEU0_TX #19 LEU0_RX #18 I2C0_SDA #19 I2C0_SCL #18	FRC_DCLK #19 FRC_DOUT #18 FRC_DFRAME #17 MODEM_DCLK #19 MODEM_DIN #18 MO-DEM_DOUT #17 MODEM_ANT0 #16 MO-DEM_ANT1 #15	PRS_CH3 #10 PRS_CH4 #2 PRS_CH5 #1 PRS_CH6 #13 ACMP0_O #19 ACMP1_O #19

		Pin Alternate Functionality / Description				
Pin #	**Pin Name**	**Analog**	**Timers**	**Communication**	**Radio**	**Other**
10	PD12	BUSCX [ADC0: APORT3XCH4 ACMP0: APORT3XCH4 ACMP1: APORT3XCH4 IDAC0: APORT1XCH4] BUSDY [ADC0: APORT4YCH4 ACMP0: APORT4YCH4 ACMP1: APORT4YCH4]	TIM0_CC0 #20 TIM0_CC1 #19 TIM0_CC2 #18 TIM0_CDTI0 #17 TIM0_CDTI1 #16 TIM0_CDTI2 #15 TIM1_CC0 #20 TIM1_CC1 #19 TIM1_CC2 #18 TIM1_CC3 #17 LE-TIM0_OUT0 #20 LETIM0_OUT1 #19 PCNT0_S0IN #20 PCNT0_S1IN #19	US0_TX #20 US0_RX #19 US0_CLK #18 US0_CS #17 US0_CTS #16 US0_RTS #15 US1_TX #20 US1_RX #19 US1_CLK #18 US1_CS #17 US1_CTS #16 US1_RTS #15 LEU0_TX #20 LEU0_RX #19 I2C0_SDA #20 I2C0_SCL #19	FRC_DCLK #20 FRC_DOUT #19 FRC_DFRAME #18 MODEM_DCLK #20 MODEM_DIN #19 MO-DEM_DOUT #18 MODEM_ANT0 #17 MO-DEM_ANT1 #16	PRS_CH3 #11 PRS_CH4 #3 PRS_CH5 #2 PRS_CH6 #14 ACMP0_O #20 ACMP1_O #20
11	PD13	BUSCY [ADC0: APORT3YCH5 ACMP0: APORT3YCH5 ACMP1: APORT3YCH5 IDAC0: APORT1YCH5] BUSDX [ADC0: APORT4XCH5 ACMP0: APORT4XCH5 ACMP1: APORT4XCH5]	TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 LE-TIM0_OUT0 #21 LETIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20	US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20	FRC_DCLK #21 FRC_DOUT #20 FRC_DFRAME #19 MODEM_DCLK #21 MODEM_DIN #20 MO-DEM_DOUT #19 MODEM_ANT0 #18 MO-DEM_ANT1 #17	PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21
12	PD14	BUSCX [ADC0: APORT3XCH6 ACMP0: APORT3XCH6 ACMP1: APORT3XCH6 IDAC0: APORT1XCH6] BUSDY [ADC0: APORT4YCH6 ACMP0: APORT4YCH6 ACMP1: APORT4YCH6]	TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 LE-TIM0_OUT0 #22 LETIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21	US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21	FRC_DCLK #22 FRC_DOUT #21 FRC_DFRAME #20 MODEM_DCLK #22 MODEM_DIN #21 MO-DEM_DOUT #20 MODEM_ANT0 #19 MO-DEM_ANT1 #18	CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 GPIO_EM4WU4

		Pin Alternate Functionality / Description				
Pin #	**Pin Name**	**Analog**	**Timers**	**Communication**	**Radio**	**Other**
13	PD15	BUSCY [ADC0: APORT3YCH7 ACMP0: APORT3YCH7 ACMP1: APORT3YCH7 IDAC0: APORT1YCH7] BUSDX [ADC0: APORT4XCH7 ACMP0: APORT4XCH7 ACMP1: APORT4XCH7]	TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 LE-TIM0_OUT0 #23 LETIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22	US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22	FRC_DCLK #23 FRC_DOUT #22 FRC_DFRAME #21 MODEM_DCLK #23 MODEM_DIN #22 MO-DEM_DOUT #21 MODEM_ANT0 #20 MO-DEM_ANT1 #19	CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 DBG_SWO #2
14	PA0	ADC0_EXTN BUSCX [ADC0: APORT3XCH8 ACMP0: APORT3XCH8 ACMP1: APORT3XCH8 IDAC0: APORT1XCH8] BUSDY [ADC0: APORT4YCH8 ACMP0: APORT4YCH8 ACMP1: APORT4YCH8]	TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 LE-TIM0_OUT0 #0 LE-TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31	US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31	FRC_DCLK #0 FRC_DOUT #31 FRC_DFRAME #30 MODEM_DCLK #0 MODEM_DIN #31 MODEM_DOUT #30 MO-DEM_ANT0 #29 MODEM_ANT1 #28	CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0
15	PA1	ADC0_EXTP BUSCY [ADC0: APORT3YCH9 ACMP0: APORT3YCH9 ACMP1: APORT3YCH9 IDAC0: APORT1YCH9] BUSDX [ADC0: APORT4XCH9 ACMP0: APORT4XCH9 ACMP1: APORT4XCH9]	TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDTI0 #30 TIM0_CDTI1 #29 TIM0_CDTI2 #28 TIM1_CC0 #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 LE-TIM0_OUT0 #1 LE-TIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0	US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0	FRC_DCLK #1 FRC_DOUT #0 FRC_DFRAME #31 MODEM_DCLK #1 MODEM_DIN #0 MODEM_DOUT #31 MO-DEM_ANT0 #30 MODEM_ANT1 #29	CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #10 PRS_CH9 #9 ACMP0_O #1 ACMP1_O #1

		Pin Alternate Functionality / Description				
Pin #	**Pin Name**	**Analog**	**Timers**	**Communication**	**Radio**	**Other**
16	PA2	BUSCX [ADC0: APORT3XCH10 ACMP0: APORT3XCH10 ACMP1: APORT3XCH10 IDAC0: APORT1XCH10] BUSDY [ADC0: APORT4YCH10 ACMP0: APORT4YCH10 ACMP1: APORT4YCH10]	TIM0_CC0 #2 TIM0_CC1 #1 TIM0_CC2 #0 TIM0_CDTI0 #31 TIM0_CDTI1 #30 TIM0_CDTI2 #29 TIM1_CC0 #2 TIM1_CC1 #1 TIM1_CC2 #0 TIM1_CC3 #31 LE-TIM0_OUT0 #2 LE-TIM0_OUT1 #1 PCNT0_S0IN #2 PCNT0_S1IN #1	US0_TX #2 US0_RX #1 US0_CLK #0 US0_CS #31 US0_CTS #30 US0_RTS #29 US1_TX #2 US1_RX #1 US1_CLK #0 US1_CS #31 US1_CTS #30 US1_RTS #29 LEU0_TX #2 LEU0_RX #1 I2C0_SDA #2 I2C0_SCL #1	FRC_DCLK #2 FRC_DOUT #1 FRC_DFRAME #0 MODEM_DCLK #2 MODEM_DIN #1 MODEM_DOUT #0 MODEM_ANT0 #31 MO-DEM_ANT1 #30	PRS_CH6 #2 PRS_CH7 #1 PRS_CH8 #0 PRS_CH9 #10 ACMP0_O #2 ACMP1_O #2
17	PA3	BUSCY [ADC0: APORT3YCH11 ACMP0: APORT3YCH11 ACMP1: APORT3YCH11 IDAC0: APORT1YCH11] BUSDX [ADC0: APORT4XCH11 ACMP0: APORT4XCH11 ACMP1: APORT4XCH11]	TIM0_CC0 #3 TIM0_CC1 #2 TIM0_CC2 #1 TIM0_CDTI0 #0 TIM0_CDTI1 #31 TIM0_CDTI2 #30 TIM1_CC0 #3 TIM1_CC1 #2 TIM1_CC2 #1 TIM1_CC3 #0 LE-TIM0_OUT0 #3 LE-TIM0_OUT1 #2 PCNT0_S0IN #3 PCNT0_S1IN #2	US0_TX #3 US0_RX #2 US0_CLK #1 US0_CS #0 US0_CTS #31 US0_RTS #30 US1_TX #3 US1_RX #2 US1_CLK #1 US1_CS #0 US1_CTS #31 US1_RTS #30 LEU0_TX #3 LEU0_RX #2 I2C0_SDA #3 I2C0_SCL #2	FRC_DCLK #3 FRC_DOUT #2 FRC_DFRAME #1 MODEM_DCLK #3 MODEM_DIN #2 MODEM_DOUT #1 MODEM_ANT0 #0 MODEM_ANT1 #31	PRS_CH6 #3 PRS_CH7 #2 PRS_CH8 #1 PRS_CH9 #0 ACMP0_O #3 ACMP1_O #3 GPIO_EM4WU8
18	PA4	BUSCX [ADC0: APORT3XCH12 ACMP0: APORT3XCH12 ACMP1: APORT3XCH12 IDAC0: APORT1XCH12] BUSDY [ADC0: APORT4YCH12 ACMP0: APORT4YCH12 ACMP1: APORT4YCH12]	TIM0_CC0 #4 TIM0_CC1 #3 TIM0_CC2 #2 TIM0_CDTI0 #1 TIM0_CDTI1 #0 TIM0_CDTI2 #31 TIM1_CC0 #4 TIM1_CC1 #3 TIM1_CC2 #2 TIM1_CC3 #1 LE-TIM0_OUT0 #4 LE-TIM0_OUT1 #3 PCNT0_S0IN #4 PCNT0_S1IN #3	US0_TX #4 US0_RX #3 US0_CLK #2 US0_CS #1 US0_CTS #0 US0_RTS #31 US1_TX #4 US1_RX #3 US1_CLK #2 US1_CS #1 US1_CTS #0 US1_RTS #31 LEU0_TX #4 LEU0_RX #3 I2C0_SDA #4 I2C0_SCL #3	FRC_DCLK #4 FRC_DOUT #3 FRC_DFRAME #2 MODEM_DCLK #4 MODEM_DIN #3 MODEM_DOUT #2 MODEM_ANT0 #1 MODEM_ANT1 #0	PRS_CH6 #4 PRS_CH7 #3 PRS_CH8 #2 PRS_CH9 #1 ACMP0_O #4 ACMP1_O #4

		Pin Alternate Functionality / Description				
Pin #	**Pin Name**	**Analog**	**Timers**	**Communication**	**Radio**	**Other**
19	PA5	BUSCY [ADC0: APORT3YCH13 ACMP0: APORT3YCH13 ACMP1: APORT3YCH13 IDAC0: APORT1YCH13] BUSDX [ADC0: APORT4XCH13 ACMP0: APORT4XCH13 ACMP1: APORT4XCH13]	TIM0_CC0 #5 TIM0_CC1 #4 TIM0_CC2 #3 TIM0_CDTI0 #2 TIM0_CDTI1 #1 TIM0_CDTI2 #0 TIM1_CC0 #5 TIM1_CC1 #4 TIM1_CC2 #3 TIM1_CC3 #2 LE-TIM0_OUT0 #5 LE-TIM0_OUT1 #4 PCNT0_S0IN #5 PCNT0_S1IN #4	US0_TX #5 US0_RX #4 US0_CLK #3 US0_CS #2 US0_CTS #1 US0_RTS #0 US1_TX #5 US1_RX #4 US1_CLK #3 US1_CS #2 US1_CTS #1 US1_RTS #0 LEU0_TX #5 LEU0_RX #4 I2C0_SDA #5 I2C0_SCL #4	FRC_DCLK #5 FRC_DOUT #4 FRC_DFRAME #3 MODEM_DCLK #5 MODEM_DIN #4 MODEM_DOUT #3 MODEM_ANT0 #2 MODEM_ANT1 #1	PRS_CH6 #5 PRS_CH7 #4 PRS_CH8 #3 PRS_CH9 #2 ACMP0_O #5 ACMP1_O #5
20	PB11	BUSCY [ADC0: APORT3YCH27 ACMP0: APORT3YCH27 ACMP1: APORT3YCH27 IDAC0: APORT1YCH27] BUSDX [ADC0: APORT4XCH27 ACMP0: APORT4XCH27 ACMP1: APORT4XCH27]	TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 LE-TIM0_OUT0 #6 LE-TIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5	US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5	FRC_DCLK #6 FRC_DOUT #5 FRC_DFRAME #4 MODEM_DCLK #6 MODEM_DIN #5 MODEM_DOUT #4 MODEM_ANT0 #3 MODEM_ANT1 #2	PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6
21	PB12	BUSCX [ADC0: APORT3XCH28 ACMP0: APORT3XCH28 ACMP1: APORT3XCH28 IDAC0: APORT1XCH28] BUSDY [ADC0: APORT4YCH28 ACMP0: APORT4YCH28 ACMP1: APORT4YCH28]	TIM0_CC0 #7 TIM0_CC1 #6 TIM0_CC2 #5 TIM0_CDTI0 #4 TIM0_CDTI1 #3 TIM0_CDTI2 #2 TIM1_CC0 #7 TIM1_CC1 #6 TIM1_CC2 #5 TIM1_CC3 #4 LE-TIM0_OUT0 #7 LE-TIM0_OUT1 #6 PCNT0_S0IN #7 PCNT0_S1IN #6	US0_TX #7 US0_RX #6 US0_CLK #5 US0_CS #4 US0_CTS #3 US0_RTS #2 US1_TX #7 US1_RX #6 US1_CLK #5 US1_CS #4 US1_CTS #3 US1_RTS #2 LEU0_TX #7 LEU0_RX #6 I2C0_SDA #7 I2C0_SCL #6	FRC_DCLK #7 FRC_DOUT #6 FRC_DFRAME #5 MODEM_DCLK #7 MODEM_DIN #6 MODEM_DOUT #5 MODEM_ANT0 #4 MODEM_ANT1 #3	PRS_CH6 #7 PRS_CH7 #6 PRS_CH8 #5 PRS_CH9 #4 ACMP0_O #7 ACMP1_O #7

		Pin Alternate Functionality / Description				
Pin #	**Pin Name**	**Analog**	**Timers**	**Communication**	**Radio**	**Other**
22	PB13	BUSCY [ADC0: APORT3YCH29 ACMP0: APORT3YCH29 ACMP1: APORT3YCH29 IDAC0: APORT1YCH29] BUSDX [ADC0: APORT4XCH29 ACMP0: APORT4XCH29 ACMP1: APORT4XCH29]	TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 LE-TIM0_OUT0 #8 LE-TIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7	US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7	FRC_DCLK #8 FRC_DOUT #7 FRC_DFRAME #6 MODEM_DCLK #8 MODEM_DIN #7 MODEM_DOUT #6 MODEM_ANT0 #5 MODEM_ANT1 #4	PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9
33	PC6	BUSAX [ADC0: APORT1XCH6 ACMP0: APORT1XCH6 ACMP1: APORT1XCH6] BUSBY [ADC0: APORT2YCH6 ACMP0: APORT2YCH6 ACMP1: APORT2YCH6]	TIM0_CC0 #11 TIM0_CC1 #10 TIM0_CC2 #9 TIM0_CDTI0 #8 TIM0_CDTI1 #7 TIM0_CDTI2 #6 TIM1_CC0 #11 TIM1_CC1 #10 TIM1_CC2 #9 TIM1_CC3 #8 LE-TIM0_OUT0 #11 LETIM0_OUT1 #10 PCNT0_S0IN #11 PCNT0_S1IN #10	US0_TX #11 US0_RX #10 US0_CLK #9 US0_CS #8 US0_CTS #7 US0_RTS #6 US1_TX #11 US1_RX #10 US1_CLK #9 US1_CS #8 US1_CTS #7 US1_RTS #6 LEU0_TX #11 LEU0_RX #10 I2C0_SDA #11 I2C0_SCL #10	FRC_DCLK #11 FRC_DOUT #10 FRC_DFRAME #9 MODEM_DCLK #11 MODEM_DIN #10 MO-DEM_DOUT #9 MODEM_ANT0 #8 MODEM_ANT1 #7	CMU_CLK0 #2 PRS_CH0 #8 PRS_CH9 #11 PRS_CH10 #0 PRS_CH11 #5 ACMP0_O #11 ACMP1_O #11
34	PC7	BUSAY [ADC0: APORT1YCH7 ACMP0: APORT1YCH7 ACMP1: APORT1YCH7] BUSBX [ADC0: APORT2XCH7 ACMP0: APORT2XCH7 ACMP1: APORT2XCH7]	TIM0_CC0 #12 TIM0_CC1 #11 TIM0_CC2 #10 TIM0_CDTI0 #9 TIM0_CDTI1 #8 TIM0_CDTI2 #7 TIM1_CC0 #12 TIM1_CC1 #11 TIM1_CC2 #10 TIM1_CC3 #9 LE-TIM0_OUT0 #12 LETIM0_OUT1 #11 PCNT0_S0IN #12 PCNT0_S1IN #11	US0_TX #12 US0_RX #11 US0_CLK #10 US0_CS #9 US0_CTS #8 US0_RTS #7 US1_TX #12 US1_RX #11 US1_CLK #10 US1_CS #9 US1_CTS #8 US1_RTS #7 LEU0_TX #12 LEU0_RX #11 I2C0_SDA #12 I2C0_SCL #11	FRC_DCLK #12 FRC_DOUT #11 FRC_DFRAME #10 MODEM_DCLK #12 MODEM_DIN #11 MO-DEM_DOUT #10 MODEM_ANT0 #9 MODEM_ANT1 #8	CMU_CLK1 #2 PRS_CH0 #9 PRS_CH9 #12 PRS_CH10 #1 PRS_CH11 #0 ACMP0_O #12 ACMP1_O #12

		Pin Alternate Functionality / Description				
Pin #	**Pin Name**	**Analog**	**Timers**	**Communication**	**Radio**	**Other**
35	PC8	BUSAX [ADC0: APORT1XCH8 ACMP0: APORT1XCH8 ACMP1: APORT1XCH8] BUSBY [ADC0: APORT2YCH8 ACMP0: APORT2YCH8 ACMP1: APORT2YCH8]	TIM0_CC0 #13 TIM0_CC1 #12 TIM0_CC2 #11 TIM0_CDTI0 #10 TIM0_CDTI1 #9 TIM0_CDTI2 #8 TIM1_CC0 #13 TIM1_CC1 #12 TIM1_CC2 #11 TIM1_CC3 #10 LE-TIM0_OUT0 #13 LETIM0_OUT1 #12 PCNT0_S0IN #13 PCNT0_S1IN #12	US0_TX #13 US0_RX #12 US0_CLK #11 US0_CS #10 US0_CTS #9 US0_RTS #8 US1_TX #13 US1_RX #12 US1_CLK #11 US1_CS #10 US1_CTS #9 US1_RTS #8 LEU0_TX #13 LEU0_RX #12 I2C0_SDA #13 I2C0_SCL #12	FRC_DCLK #13 FRC_DOUT #12 FRC_DFRAME #11 MODEM_DCLK #13 MODEM_DIN #12 MO-DEM_DOUT #11 MODEM_ANT0 #10 MO-DEM_ANT1 #9	PRS_CH0 #10 PRS_CH9 #13 PRS_CH10 #2 PRS_CH11 #1 ACMP0_O #13 ACMP1_O #13
36	PC9	BUSAY [ADC0: APORT1YCH9 ACMP0: APORT1YCH9 ACMP1: APORT1YCH9] BUSBX [ADC0: APORT2XCH9 ACMP0: APORT2XCH9 ACMP1: APORT2XCH9]	TIM0_CC0 #14 TIM0_CC1 #13 TIM0_CC2 #12 TIM0_CDTI0 #11 TIM0_CDTI1 #10 TIM0_CDTI2 #9 TIM1_CC0 #14 TIM1_CC1 #13 TIM1_CC2 #12 TIM1_CC3 #11 LE-TIM0_OUT0 #14 LETIM0_OUT1 #13 PCNT0_S0IN #14 PCNT0_S1IN #13	US0_TX #14 US0_RX #13 US0_CLK #12 US0_CS #11 US0_CTS #10 US0_RTS #9 US1_TX #14 US1_RX #13 US1_CLK #12 US1_CS #11 US1_CTS #10 US1_RTS #9 LEU0_TX #14 LEU0_RX #13 I2C0_SDA #14 I2C0_SCL #13	FRC_DCLK #14 FRC_DOUT #13 FRC_DFRAME #12 MODEM_DCLK #14 MODEM_DIN #13 MO-DEM_DOUT #12 MODEM_ANT0 #11 MO-DEM_ANT1 #10	PRS_CH0 #11 PRS_CH9 #14 PRS_CH10 #3 PRS_CH11 #2 ACMP0_O #14 ACMP1_O #14
37	PC10	BUSAX [ADC0: APORT1XCH10 ACMP0: APORT1XCH10 ACMP1: APORT1XCH10] BUSBY [ADC0: APORT2YCH10 ACMP0: APORT2YCH10 ACMP1: APORT2YCH10]	TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 LE-TIM0_OUT0 #15 LETIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14	US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14	FRC_DCLK #15 FRC_DOUT #14 FRC_DFRAME #13 MODEM_DCLK #15 MODEM_DIN #14 MO-DEM_DOUT #13 MODEM_ANT0 #12 MO-DEM_ANT1 #11	CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 GPIO_EM4WU12

		Pin Alternate Functionality / Description				
Pin #	**Pin Name**	**Analog**	**Timers**	**Communication**	**Radio**	**Other**
38	PC11	BUSAY [ADC0: APORT1YCH11 ACMP0: APORT1YCH11 ACMP1: APORT1YCH11] BUSBX [ADC0: APORT2XCH11 ACMP0: APORT2XCH11 ACMP1: APORT2XCH11]	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 LE-TIM0_OUT0 #16 LETIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15	FRC_DCLK #16 FRC_DOUT #15 FRC_DFRAME #14 MODEM_DCLK #16 MODEM_DIN #15 MO-DEM_DOUT #14 MODEM_ANT0 #13 MO-DEM_ANT1 #12	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3
39	PF0	BUSAX [ADC0: APORT1XCH16 ACMP0: APORT1XCH16 ACMP1: APORT1XCH16] BUSBY [ADC0: APORT2YCH16 ACMP0: APORT2YCH16 ACMP1: APORT2YCH16]	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 LE-TIM0_OUT0 #24 LETIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	FRC_DCLK #24 FRC_DOUT #23 FRC_DFRAME #22 MODEM_DCLK #24 MODEM_DIN #23 MO-DEM_DOUT #22 MODEM_ANT0 #21 MO-DEM_ANT1 #20	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK #0
40	PF1	BUSAY [ADC0: APORT1YCH17 ACMP0: APORT1YCH17 ACMP1: APORT1YCH17] BUSBX [ADC0: APORT2XCH17 ACMP0: APORT2XCH17 ACMP1: APORT2XCH17]	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 LE-TIM0_OUT0 #25 LETIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	FRC_DCLK #25 FRC_DOUT #24 FRC_DFRAME #23 MODEM_DCLK #25 MODEM_DIN #24 MO-DEM_DOUT #23 MODEM_ANT0 #22 MO-DEM_ANT1 #21	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS #0

		Pin Alternate Functionality / Description				
Pin #	**Pin Name**	**Analog**	**Timers**	**Communication**	**Radio**	**Other**
41	PF2	BUSAX [ADC0: APORT1XCH18 ACMP0: APORT1XCH18 ACMP1: APORT1XCH18] BUSBY [ADC0: APORT2YCH18 ACMP0: APORT2YCH18 ACMP1: APORT2YCH18]	TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 LE-TIM0_OUT0 #26 LETIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25	US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25	FRC_DCLK #26 FRC_DOUT #25 FRC_DFRAME #24 MODEM_DCLK #26 MODEM_DIN #25 MO-DEM_DOUT #24 MODEM_ANT0 #23 MO-DEM_ANT1 #22	CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO #0 DBG_SWO #0 GPIO_EM4WU0
42	PF3	BUSAY [ADC0: APORT1YCH19 ACMP0: APORT1YCH19 ACMP1: APORT1YCH19] BUSBX [ADC0: APORT2XCH19 ACMP0: APORT2XCH19 ACMP1: APORT2XCH19]	TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 LE-TIM0_OUT0 #27 LETIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26	US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26	FRC_DCLK #27 FRC_DOUT #26 FRC_DFRAME #25 MODEM_DCLK #27 MODEM_DIN #26 MO-DEM_DOUT #25 MODEM_ANT0 #24 MO-DEM_ANT1 #23	CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI #0
43	PF4	BUSAX [ADC0: APORT1XCH20 ACMP0: APORT1XCH20 ACMP1: APORT1XCH20] BUSBY [ADC0: APORT2YCH20 ACMP0: APORT2YCH20 ACMP1: APORT2YCH20]	TIM0_CC0 #28 TIM0_CC1 #27 TIM0_CC2 #26 TIM0_CDTI0 #25 TIM0_CDTI1 #24 TIM0_CDTI2 #23 TIM1_CC0 #28 TIM1_CC1 #27 TIM1_CC2 #26 TIM1_CC3 #25 LE-TIM0_OUT0 #28 LETIM0_OUT1 #27 PCNT0_S0IN #28 PCNT0_S1IN #27	US0_TX #28 US0_RX #27 US0_CLK #26 US0_CS #25 US0_CTS #24 US0_RTS #23 US1_TX #28 US1_RX #27 US1_CLK #26 US1_CS #25 US1_CTS #24 US1_RTS #23 LEU0_TX #28 LEU0_RX #27 I2C0_SDA #28 I2C0_SCL #27	FRC_DCLK #28 FRC_DOUT #27 FRC_DFRAME #26 MODEM_DCLK #28 MODEM_DIN #27 MO-DEM_DOUT #26 MODEM_ANT0 #25 MO-DEM_ANT1 #24	PRS_CH0 #4 PRS_CH1 #3 PRS_CH2 #2 PRS_CH3 #1 ACMP0_O #28 ACMP1_O #28

		Pin Alternate Functionality / Description				
Pin #	**Pin Name**	**Analog**	**Timers**	**Communication**	**Radio**	**Other**
44	PF5	BUSAY [ADC0: APORT1YCH21 ACMP0: APORT1YCH21 ACMP1: APORT1YCH21] BUSBX [ADC0: APORT2XCH21 ACMP0: APORT2XCH21 ACMP1: APORT2XCH21]	TIM0_CC0 #29 TIM0_CC1 #28 TIM0_CC2 #27 TIM0_CDTI0 #26 TIM0_CDTI1 #25 TIM0_CDTI2 #24 TIM1_CC0 #29 TIM1_CC1 #28 TIM1_CC2 #27 TIM1_CC3 #26 LE-TIM0_OUT0 #29 LETIM0_OUT1 #28 PCNT0_S0IN #29 PCNT0_S1IN #28	US0_TX #29 US0_RX #28 US0_CLK #27 US0_CS #26 US0_CTS #25 US0_RTS #24 US1_TX #29 US1_RX #28 US1_CLK #27 US1_CS #26 US1_CTS #25 US1_RTS #24 LEU0_TX #29 LEU0_RX #28 I2C0_SDA #29 I2C0_SCL #28	FRC_DCLK #29 FRC_DOUT #28 FRC_DFRAME #27 MODEM_DCLK #29 MODEM_DIN #28 MO-DEM_DOUT #27 MODEM_ANT0 #26 MO-DEM_ANT1 #25	PRS_CH0 #5 PRS_CH1 #4 PRS_CH2 #3 PRS_CH3 #2 ACMP0_O #29 ACMP1_O #29
45	PF6	BUSAX [ADC0: APORT1XCH22 ACMP0: APORT1XCH22 ACMP1: APORT1XCH22] BUSBY [ADC0: APORT2YCH22 ACMP0: APORT2YCH22 ACMP1: APORT2YCH22]	TIM0_CC0 #30 TIM0_CC1 #29 TIM0_CC2 #28 TIM0_CDTI0 #27 TIM0_CDTI1 #26 TIM0_CDTI2 #25 TIM1_CC0 #30 TIM1_CC1 #29 TIM1_CC2 #28 TIM1_CC3 #27 LE-TIM0_OUT0 #30 LETIM0_OUT1 #29 PCNT0_S0IN #30 PCNT0_S1IN #29	US0_TX #30 US0_RX #29 US0_CLK #28 US0_CS #27 US0_CTS #26 US0_RTS #25 US1_TX #30 US1_RX #29 US1_CLK #28 US1_CS #27 US1_CTS #26 US1_RTS #25 LEU0_TX #30 LEU0_RX #29 I2C0_SDA #30 I2C0_SCL #29	FRC_DCLK #30 FRC_DOUT #29 FRC_DFRAME #28 MODEM_DCLK #30 MODEM_DIN #29 MO-DEM_DOUT #28 MODEM_ANT0 #27 MO-DEM_ANT1 #26	CMU_CLK1 #7 PRS_CH0 #6 PRS_CH1 #5 PRS_CH2 #4 PRS_CH3 #3 ACMP0_O #30 ACMP1_O #30
46	PF7	BUSAY [ADC0: APORT1YCH23 ACMP0: APORT1YCH23 ACMP1: APORT1YCH23] BUSBX [ADC0: APORT2XCH23 ACMP0: APORT2XCH23 ACMP1: APORT2XCH23]	TIM0_CC0 #31 TIM0_CC1 #30 TIM0_CC2 #29 TIM0_CDTI0 #28 TIM0_CDTI1 #27 TIM0_CDTI2 #26 TIM1_CC0 #31 TIM1_CC1 #30 TIM1_CC2 #29 TIM1_CC3 #28 LE-TIM0_OUT0 #31 LETIM0_OUT1 #30 PCNT0_S0IN #31 PCNT0_S1IN #30	US0_TX #31 US0_RX #30 US0_CLK #29 US0_CS #28 US0_CTS #27 US0_RTS #26 US1_TX #31 US1_RX #30 US1_CLK #29 US1_CS #28 US1_CTS #27 US1_RTS #26 LEU0_TX #31 LEU0_RX #30 I2C0_SDA #31 I2C0_SCL #30	FRC_DCLK #31 FRC_DOUT #30 FRC_DFRAME #29 MODEM_DCLK #31 MODEM_DIN #30 MO-DEM_DOUT #29 MODEM_ANT0 #28 MO-DEM_ANT1 #27	CMU_CLK0 #7 PRS_CH0 #7 PRS_CH1 #6 PRS_CH2 #5 PRS_CH3 #4 ACMP0_O #31 ACMP1_O #31 GPIO_EM4WU1

7.1.1 GPIO Overview

The GPIO pins are organized as 16-bit ports indicated by letters A through F, and the individual pins on each port are indicated by a number from 15 down to 0.

Table 7.2. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	PA5 (5V)	PA4 (5V)	PA3 (5V)	PA2 (5V)	PA1	PA0
Port B			PB13 [2] (5V)	PB12 [2](5V)	PB11 [2] (5V)	-	-	-	-	-	-	-	-	-	-	-
Port C	-	-	-	-	PC11 (5V)	PC10 (5V)	PC9 (5V)	PC8 (5V)	PC7 (5V)	PC6 (5V)	-	-	-	-	-	-
Port D	PD15 [2] (5V)	PD14 [2] (5V)	PD13 [2] (5V)	PD12 (5V)	PD11 (5V)	PD10 (5V)	PD9 (5V)	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	PF7 (5V)	PF6 (5V)	PF5 (5V)	PF4 (5V)	PF3 (5V)	PF2 (5V)	PF1 (5V)	PF0 (5V)

Note:

1. GPIO with 5V compatibility are indicated by (5V)
2. Pins PA2, PA3, PA4, PB11, PB12, PD13, PD14 and PD15 will not be 5V compatible on all future devices.

In order to preserve upgrade options with full hardware compatibility, do not use the pins listed in Note 2 with 5V domains.

7.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 7.3. Alternate functionality overview

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
ACMP0_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP0, digital output.
ACMP1_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP1, digital output.
ADC0_EXTN	0: PA0								Analog to digital converter ADC0 external reference input negative pin
ADC0_EXTP	0: PA1								Analog to digital converter ADC0 external reference input positive pin
CMU_CLK0	0: PA1 2: PC6 3: PC11	4: PD9 5: PD14 6: PF2 7: PF7							Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA0 2: PC7 3: PC10	4: PD10 5: PD15 6: PF3 7: PF6							Clock Management Unit, clock output number 1.
DBG_SWCLKTCK	0: PF0								Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.
DBG_SWDIOTMS	0: PF1								Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
DBG_SWO	0: PF2 1: PB13 2: PD15 3: PC11								Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
DBG_TDI	0: PF3								Debug-interface JTAG Test Data In. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_TDO	0: PF2								Debug-interface JTAG Test Data Out. Note that this function is enabled to pin out of reset.
FRC_DCLK	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Frame Controller, Data Sniffer Clock.
FRC_DFRAME	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13	9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Frame Controller, Data Sniffer Frame active
FRC_DOUT	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	17: PD10 18: PD11 19:PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Frame Controller, Data Sniffer Output.
GPIO_EM4WU0	0: PF2								Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PF7								Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PD14								Pin can be used to wake the system up from EM4
GPIO_EM4WU8	0: PA3								Pin can be used to wake the system up from EM4
GPIO_EM4WU9	0: PB13								Pin can be used to wake the system up from EM4

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
GPIO_EM4WU12	0: PC10								Pin can be used to wake the system up from EM4
I2C0_SCL	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	I2C0 Serial Clock Line input / output.
I2C0_SDA	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	I2C0 Serial Data input / output.
LETIM0_OUT0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 11: PC6	12: PC8 13: PC9 14: PC10 15: PC11	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	LEUART0 Receive input.
LEU0_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N									Connected internally to a Low Frequency Crystal (32.768 kHz). Leave unconnected externally.
LFXTAL_P									Connected internally to a Low Frequency Crystal (32.768 kHz). Leave unconnected externally.
MODEM_ANT0	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	MODEM antenna control output 0, used for antenna diversity.
MODEM_ANT1	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 7: PC6	8: PC7 9: PC8 10: PC9 11: PC11	12: PC11 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	MODEM antenna control output 1, used for antenna diversity.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
MODEM_DCLK	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	MODEM data clock out.
MODEM_DIN	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	MODEM data in.
MODEM_DOUT	0: PA2 1: PA3 2: PA4 3:PA5	4: PB11 5: PB12 6: PB13	9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	MODEM data out.
PCNT0_S0IN	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Pulse Counter PCNT0 input number 1.
PRS_CH0	0: PF0 1: PF1 2: PF2 3: PF3	4: PF4 5: PF5 6: PF6 7: PF7	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11					Peripheral Reflex System PRS, channel 0.
PRS_CH1	0: PF1 1: PF2 2: PF3 3: PF4	4: PF5 5: PF6 6: PF7 7: PF0							Peripheral Reflex System PRS, channel 1.
PRS_CH2	0: PF2 1: PF3 2: PF4 3: PF5	4: PF6 5: PF7 6: PF0 7: PF1							Peripheral Reflex System PRS, channel 2.
PRS_CH3	0: PF3 1: PF4 2: PF5 3: PF6	4: PF7 5: PF0 6: PF1 7: PF2	8: PD9 9: PD10 10: PD11 11: PD12	12: PD13 13: PD14 14: PD15					Peripheral Reflex System PRS, channel 3.
PRS_CH4	0: PD9 1: PD10 2: PD11 3: PD12	4: PD13 5: PD14 6: PD15							Peripheral Reflex System PRS, channel 4.
PRS_CH5	0: PD10 1: PD11 2: PD12 3: PD13	4: PD14 5: PD15 6: PD9							Peripheral Reflex System PRS, channel 5.
PRS_CH6	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5. PA5 6: PB11 7: PB12	8: PB13 11: PD9	12: PD10 13: PD11 14: PD12 15: PD13	16: PD14 17: PD15				Peripheral Reflex System PRS, channel 6.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
PRS_CH7	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	10: PA0						Peripheral Reflex System PRS, channel 7.
PRS_CH8	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13	9: PA0 10: PA1						Peripheral Reflex System PRS, channel 8.
PRS_CH9	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13	8: PA0 9: PA1 10: PA2 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11				Peripheral Reflex System PRS, channel 9.
PRS_CH10	0: PC6 1: PC7 2: PC8 3: PC9	4: PC10 5: PC11							Peripheral Reflex System PRS, channel 10.
PRS_CH11	0: PC7 1: PC8 2: PC9 3: PC10	4: PC11 5: PC6							Peripheral Reflex System PRS, channel 11.
TIM0_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF12 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13	9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 0 Complimentary Dead Time Insertion channel 0.
TIM0_CDTI1	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	Timer 0 Complimentary Dead Time Insertion channel 1.
TIM0_CDTI2	0: PA5 1: PB11 2: PB12 3: PB13	6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	12: PD9 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	Timer 0 Complimentary Dead Time Insertion channel 2.
TIM1_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 1 Capture Compare input / output channel 0.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
TIM1_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 225: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13	9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 1 Capture Compare input / output channel 2.
TIM1_CC3	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 1 Capture Compare input / output channel 3.
US0_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13	9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART0 clock input / output.
US0_CS	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART0 chip select input / output.
US0_CTS	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART0 Clear To Send hardware flow control input.
US0_RTS	0: PA5 1: PB11 2: PB12 3: PB13	6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	12: PD9 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART0 Request To Send hardware flow control output.
US0_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13	9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART1 clock input / output.
US1_CS	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART1 chip select input / output.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
US1_CTS	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART1 Clear To Send hardware flow control input.
US1_RTS	0: PA5 1: PB11 2: PB12 3: PB13	6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	12: PD9 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART1 Request To Send hardware flow control output.
US1_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

7.3 Analog Port (APORT)

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, and DACs. The APORT consists of wires, switches, and control needed to configurably implement the routes. Please see the device Reference Manual for a complete description.

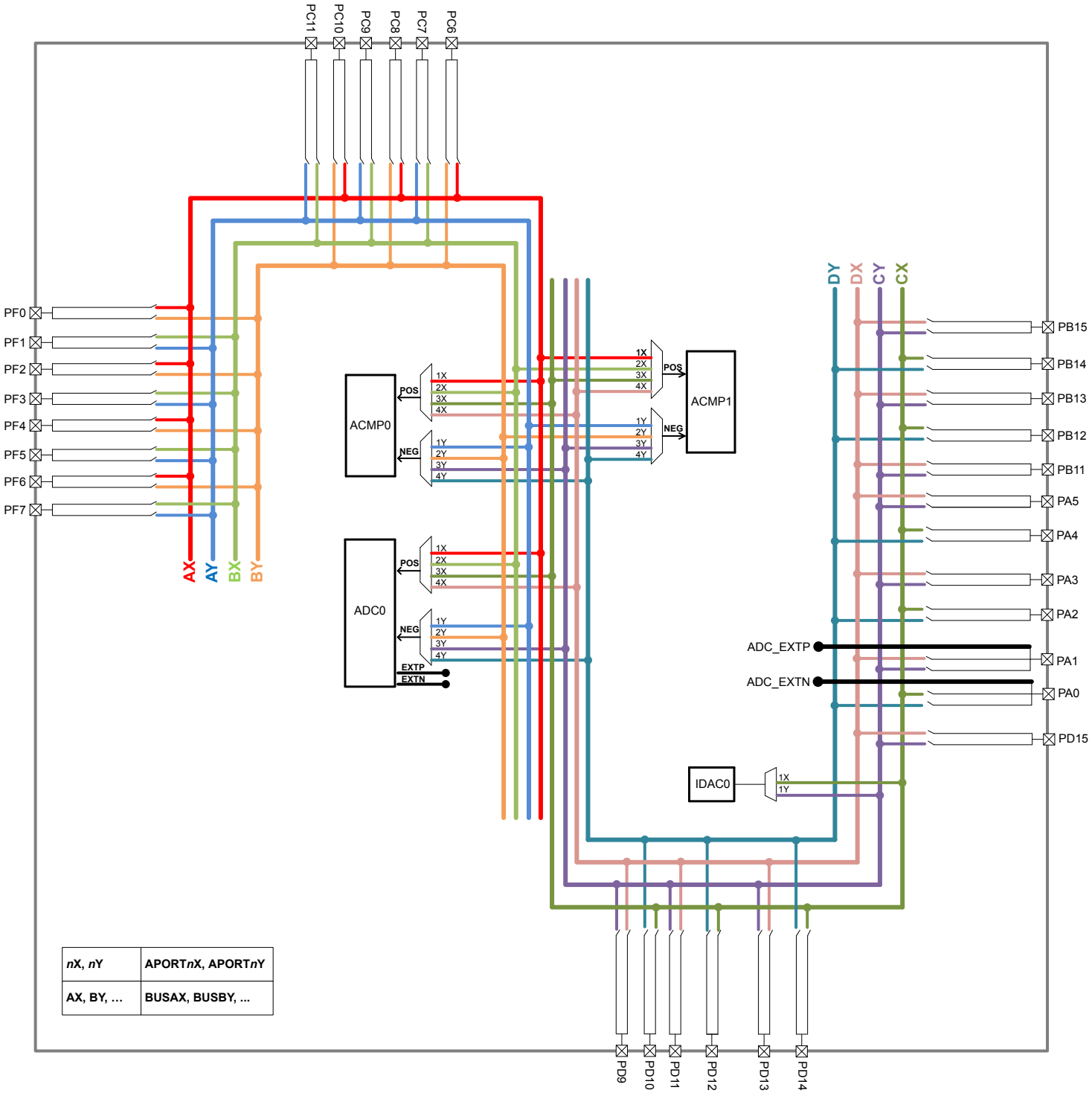


Figure 7.2. BGM11S APORT

Table 7.4. ACMP0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSAX										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2X	BUSBX									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4X	BUSDX	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		

Table 7.5. ACMP1 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSAX										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2X	BUSBX									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4X	BUSDX	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		

Table 7.6. ADC0 Bus and Pin Mapping

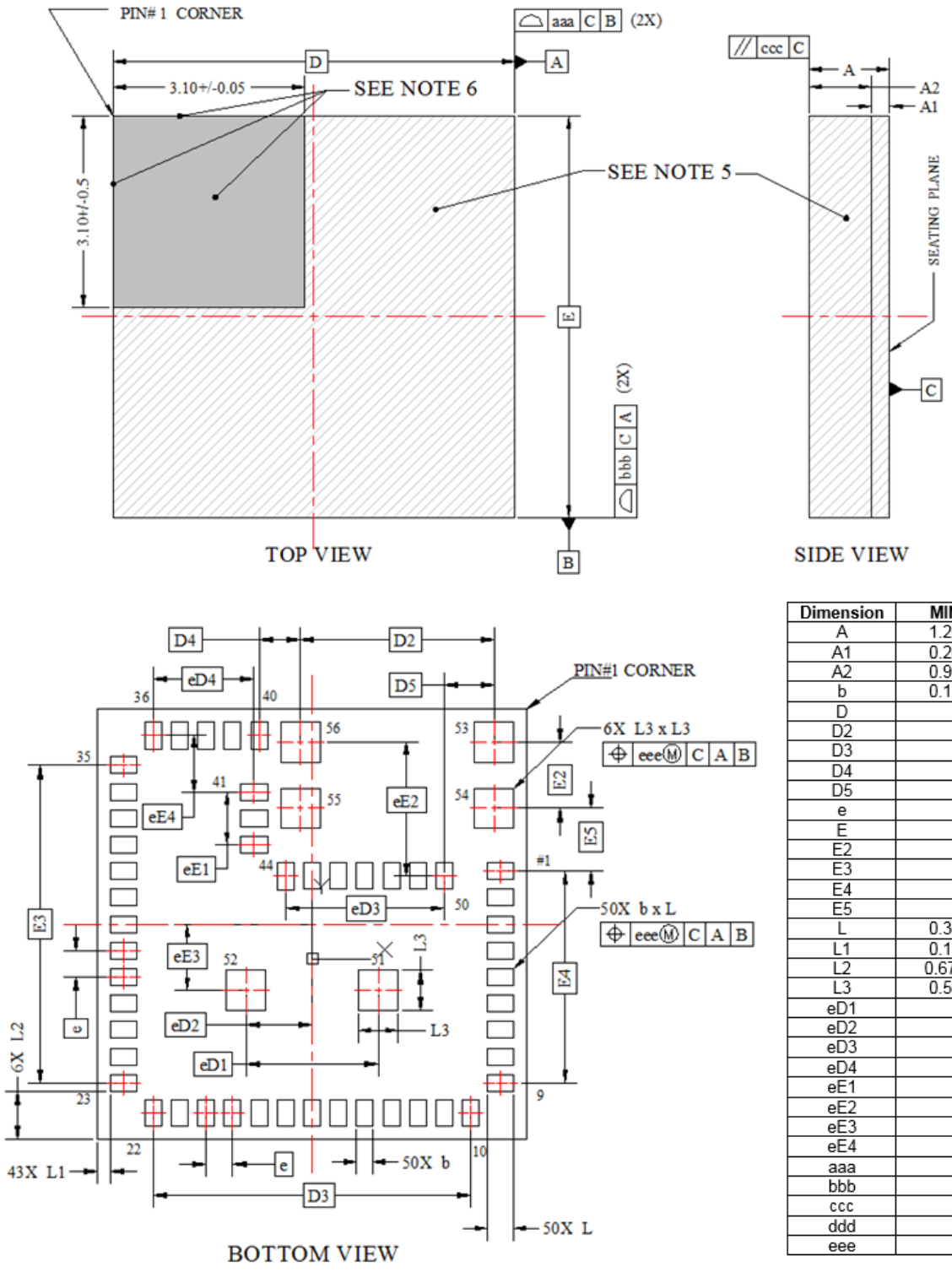
Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSAX										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2X	BUSBX									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4X	BUSDX	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		

Table 7.7. IDAC0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT1Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	

8. Package Specifications

8.1 BGM11S Package Dimensions



Dimension	MIN	NOM	MAX
A	1.20	1.30	1.40
A1	0.26	0.30	0.34
A2	0.95	1.00	1.05
b	0.15	0.25	0.35
D		6.50 BSC	
D2		2.925 BSC	
D3		4.80 BSC	
D4		0.625 BSC	
D5		0.75 BSC	
e		0.40 BSC	
E		6.50 BSC	
E2		1.00 BSC	
E3		4.80 BSC	
E4		3.20 BSC	
E5		0.95 BSC	
L	0.30	0.40	0.50
L1	0.15	0.20	0.25
L2	0.675	0.725	0.775
L3	0.50	0.60	0.70
eD1		2.00 BSC	
eD2		1.00 BSC	
eD3		2.40 BSC	
eD4		1.525 BSC	
eE1		0.80 BSC	
eE2		2.025 BSC	
eE3		1.00 BSC	
eE4		0.85 BSC	
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.10	
eee		0.10	

Figure 8.1. BGM11S Package Dimensions

Table 8.1. Package Dimensions

Dimension	MIN	NOM	MAX
A	1.20	1.30	1.40
A1	0.26	0.30	0.34
A2	0.95	1.00	1.05
b	0.15	0.25	0.35
D	6.50 BSC		
D2	2.925 BSC		
D3	4.80 BSC		
D4	0.625 BSC		
D5	0.75 BSC		
e	0.40 BSC		
E	6.50 BSC		
E2	1.00 BSC		
E3	4.80 BSC		
E4	3.20 BSC		
E5	0.95 BSC		
L	0.30	0.40	0.50
L1	0.15	0.20	0.25
L2	0.675	0.725	0.775
L3	0.50	0.60	0.70
eD1	2.00 BSC		
eD2	1.00 BSC		
eD3	2.40 BSC		
eD4	1.525 BSC		
eE1	0.80 BSC		
eE2	2.025 BSC		
eE3	1.00 BSC		
eE4	0.85 BSC		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.10		
eee	0.10		

Dimension	MIN	NOM	MAX

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
5. Solid pattern (3.1mm x 3.1mm) shows non-shielding area including its side walls. For side wall, borderline between shielding area and not-shielding area could not be defined clearly like top side.

8.2 BGM11S Package Marking

The figure below shows the package markings printed on the module.

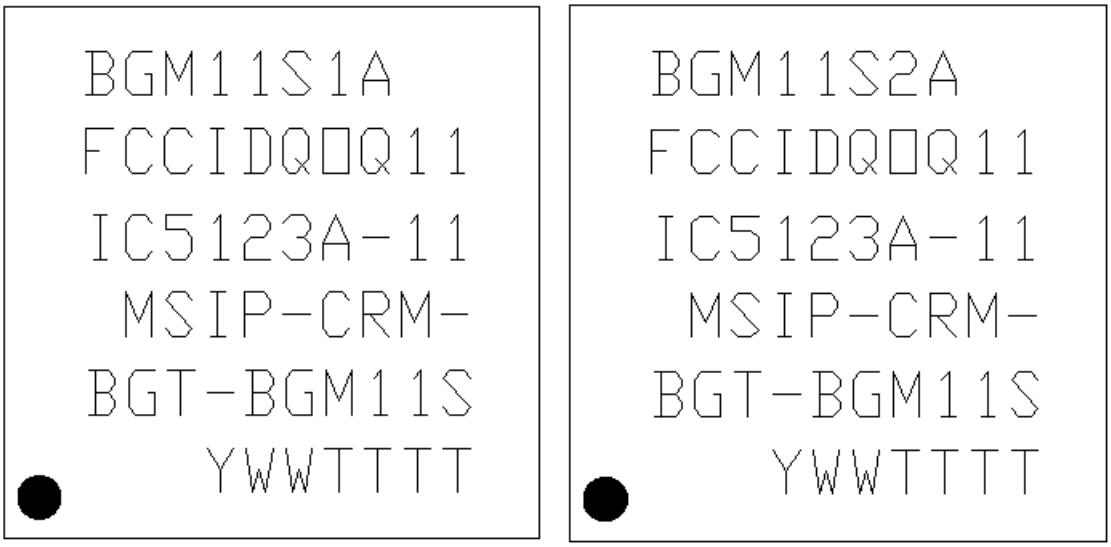


Figure 8.2. BGM11S Package Marking

Table 8.2. Explanations

Marking	Explanation
BGM11S1A	The part number designation 1. Family Code (B=Blue) 2. G (Gecko) 3. M (Module) 4. Series (1,2,...) 5. Device Configuration (1,2,...) 6. Module Type (S= SiP Module, P= PCB Module) 7. TX Output Power (1=Low, 2=Medium, 3=High) 8. Antenna Type (A = Internal chip Antenna, N = RF PIN)
FCCIDQ0Q11	FCC Certification ID
IC5123A-11	IC5123A-11
MSIP-CRM-BGT-11	KC (Korea) Certification ID
YWWTTTT	1. Y = Manufacturing Year 2. WW = Manufacturing Work Week 3. TTTT = Trace Code

8.3 BGM11S Recommended PCB Land Pattern

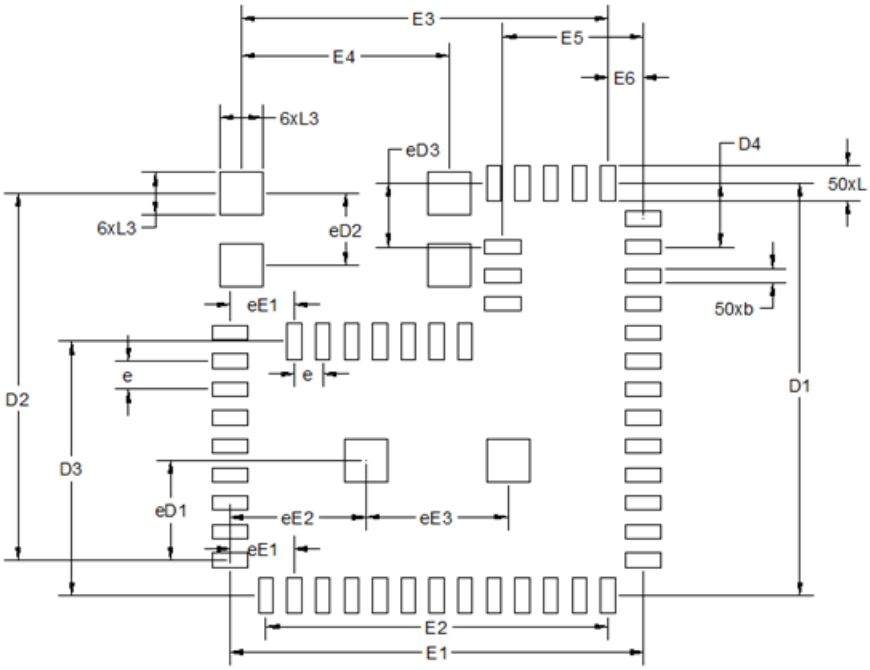


Figure 8.3. Module Footprint

Table 8.3. PCB Land Pattern Dimensions

Symbol	NOM (mm)
b	0.20 BSC
D1	5.80 BSC
D2	5.150 BSC
D3	3.575 BSC
D4	0.90 BSC
e	0.400 BSC
E1	5.800 BSC
E2	4.800 BSC
E3	5.150 BSC
E4	2.925 BSC
E5	1.975 BSC
E6	0.50 BSC
L	0.50 BSC
L3	0.60 BSC
eD1	1.40 BSC
eD2	1.00 BSC
eD3	0.90 BSC

Symbol	NOM (mm)
eE1	0.90 BSC
eE2	1.90 BSC
eE3	2.00 BSC

Note:

1. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05mm is assumed.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.

   Note: Soldering process specific adjustments may need to be made to the PCB land pattern.
4. The smaller rectangle pads are longer and thinner on the PCB Land Pattern(LPD) than the Package Outline Drawing(POD) (0.2 x 0.5 vs. 0.25 x 0.4). The LPD pad edge aligns with the edge of the POD pads. The centers of the respective pads do not align and that is the cause of the dimensional differences between POD and LPD.
5. Above notes and stencil design are shared as recommendations only. A user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.

ANTENNA LAYOUT RECOMMENDATION

This section describes the recommended PCB land pattern for the BGM11S with X-Y cordinates of pads and the antenna copper clearance area. The X-Y cordinates of pads relative to the origo are shown in the table. The origo is the center point of pin no 53. It is very important to align the antenna area relative to the module pads precisely. This recommendation is only valid for parts with built-in antenna.

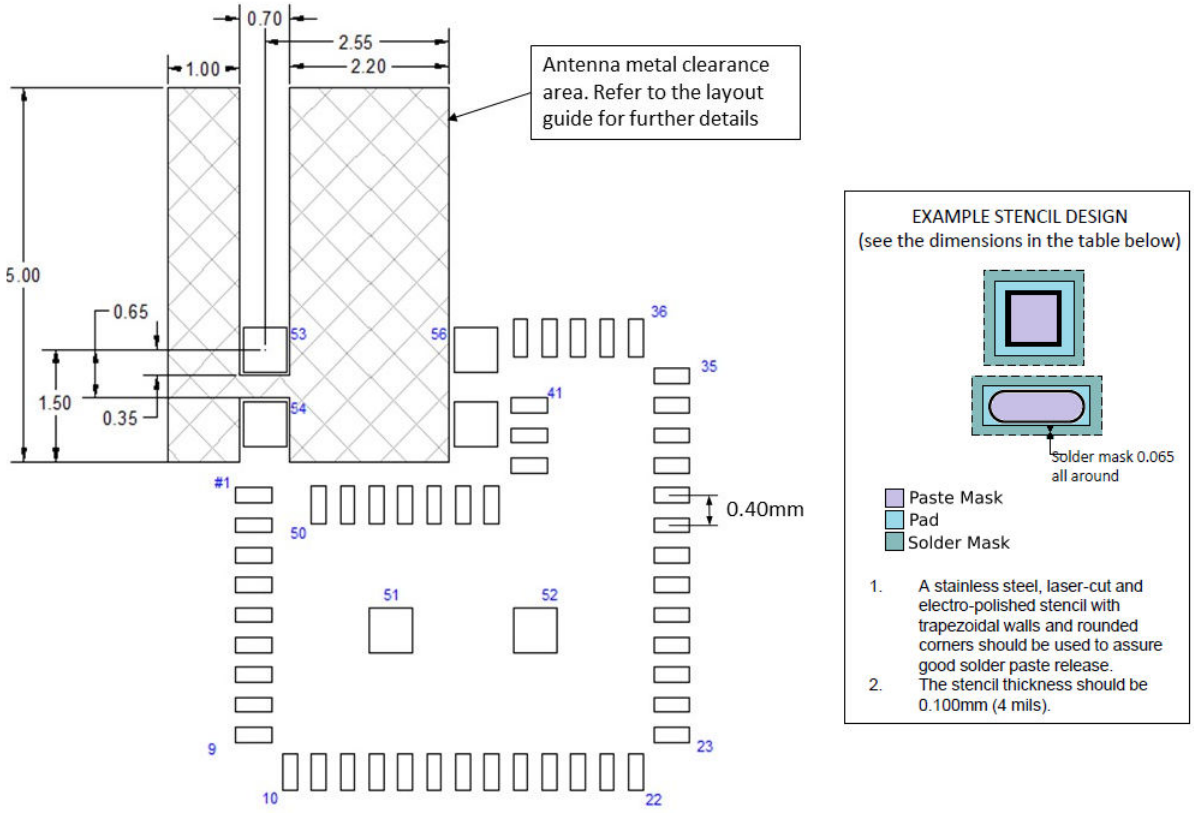


Figure 8.4. BGM11S Recommended Land Pattern

Note: The provided stencil information is a recommendation and soldering process specific adjustments may need to be made.

Table 8.4. Layout Recommendation

Pad No.	Pad coordinates (X,Y)	Pad size (mm)	Solder mask opening size (mm)	Stencil aperture size (mm)
53	(0,0)	0.6 x 0.6	0.73 x 0.73	0.48 x 0.48
51	(1.75, -3.75)			
52	(3.75,-3.75)			
54	(0,-1.0)			
56	(2.925,0)			

Pad No.	Pad coordinates (X,Y)	Pad size (mm)	Solder mask opening size (mm)	Stencil aperture size (mm)
1	(-0.15,-1.95)	0.20 x 0.50	0.33 x 0.63	0.20 x 0.45
9	(-0.15,-5.15)			
10	(0.35,-5.65)			
22	(5.15,-5.65)			
23	(5.65,-5.15)			
35	(5.65,-0.35)			
36	(5.15,0.15)			
41	(3.675,-0.75)			
50	(0.75,-2.075)			

9. Tape and Reel Specifications

9.1 Tape and Reel Packaging

This section contains information regarding the tape and reel packaging for the BGM11S Blue Gecko Module.

9.2 Reel and Tape Specifications

- Reel material: Polystyrene (PS)
- Reel diameter: 13 inches (330 mm)
- Number of modules per reel: 1000 pcs
- Disk deformation, folding whitening and mold imperfections: Not allowed
- Disk set: consists of two 13 inch (330 mm) rotary round disks and one central axis (100 mm)
- Antistatic treatment: Required
- Surface resistivity: 10^4 - 10^9 Ω/sq.

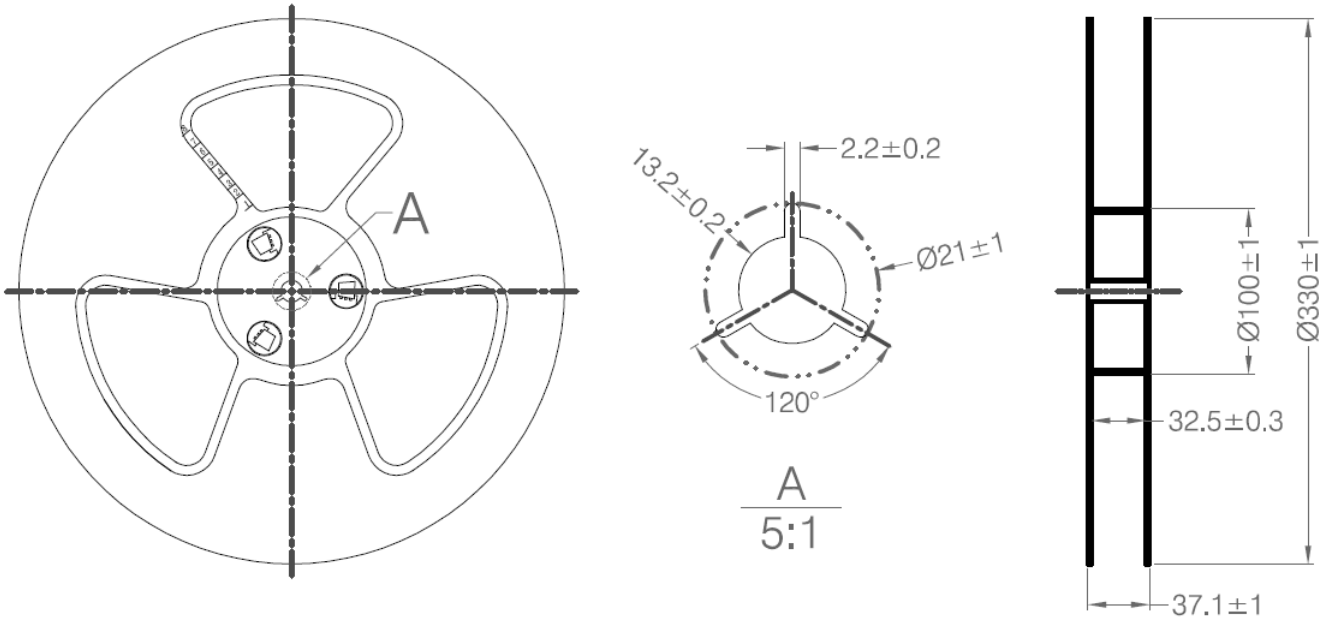


Figure 9.1. Reel Dimensions - Side View

Table 9.1. Reel Dimensions

Symbol	Dimensions [mm]
W0	32.5 ± 0.3
W1	37.1 ± 1.0

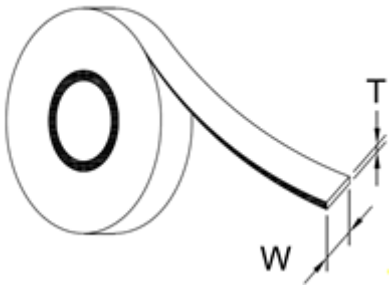


Figure 9.2. Cover tape information

Table 9.2. Cover Tape Dimensions

Symbol	Dimensions [mm]
Thickness (T)	0.061
Width (W)	25.5 + 0.2

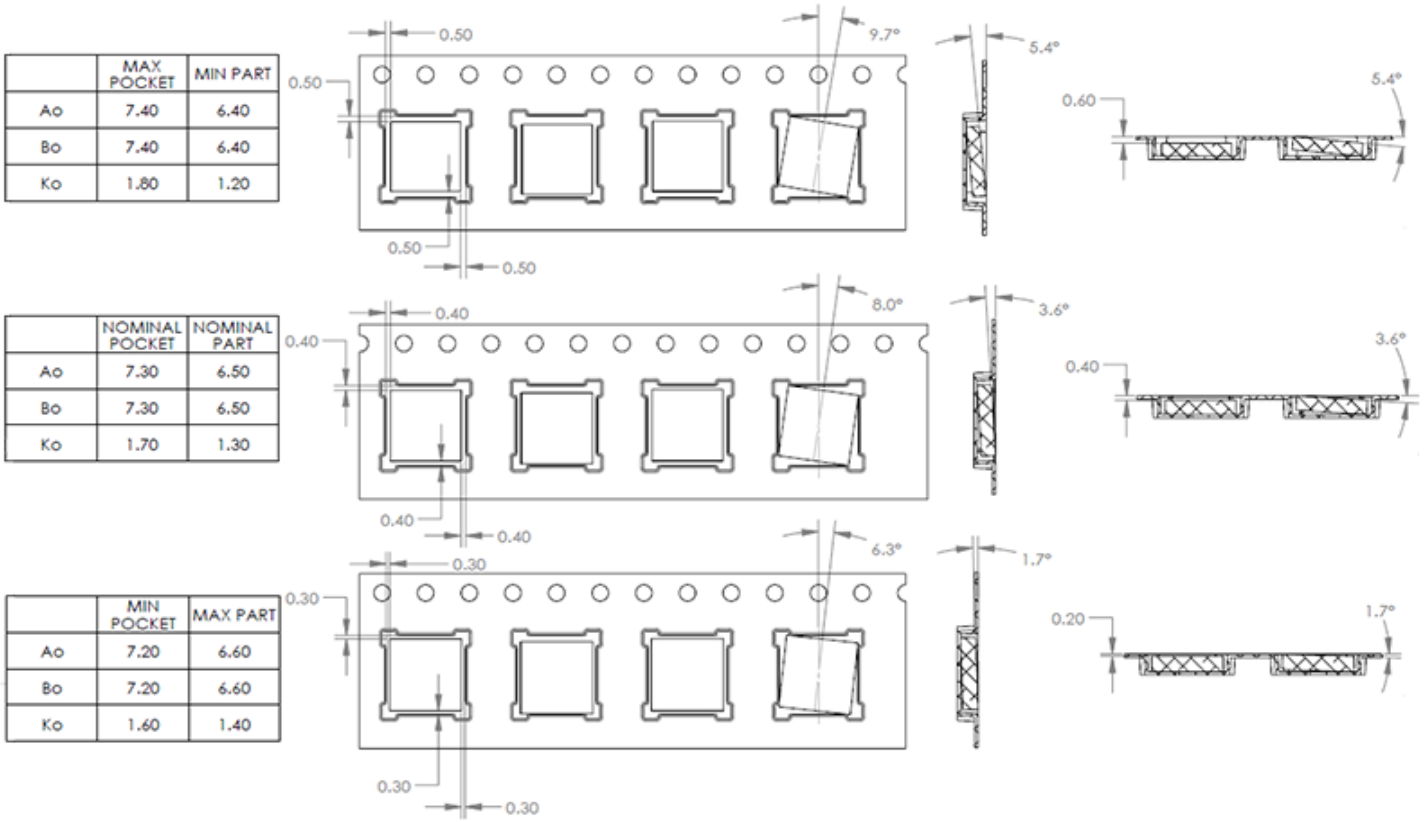


Figure 9.3. Tape information

9.3 Orientation and Tape Feed

The user direction of feed, start and end of tape on reel and orientation of the Modules on the tape are shown in the figures below.

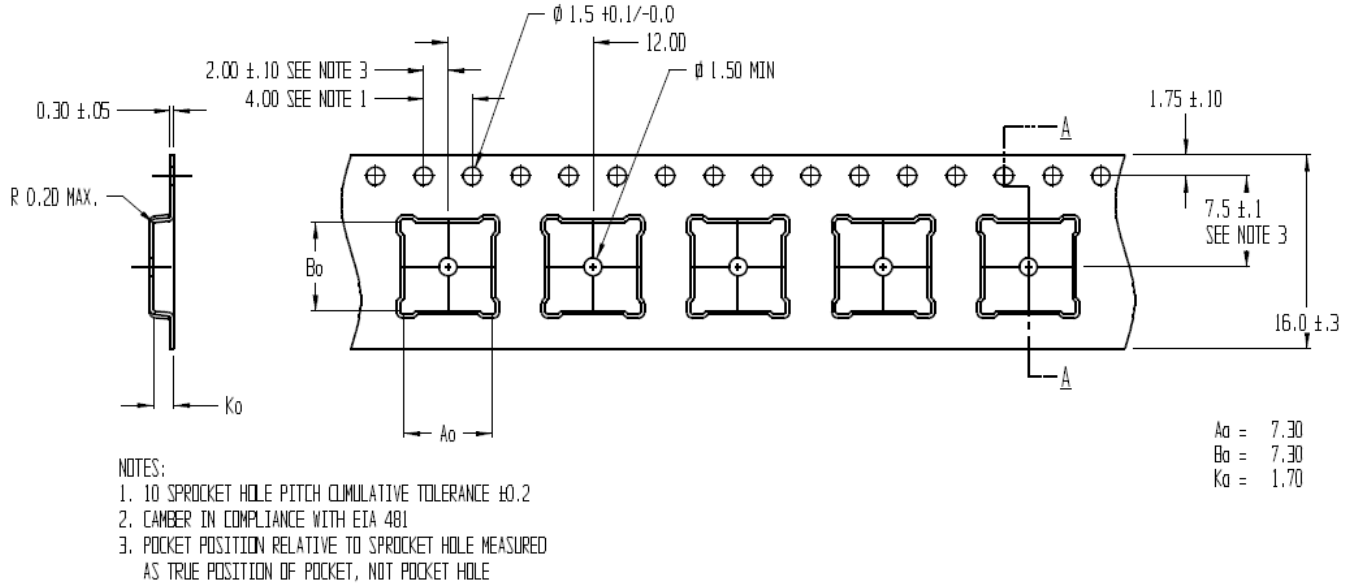


Figure 9.4. Module Orientation and Feed Direction

9.4 Tape and Reel Box Dimensions

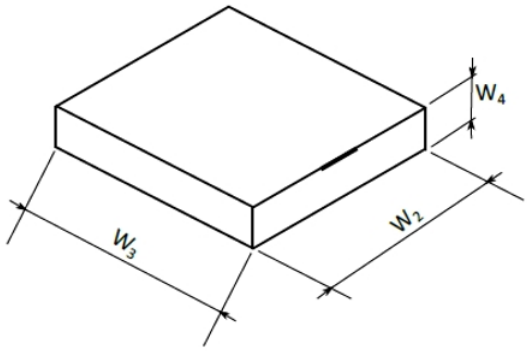


Figure 9.5. Tape and Reel Box Dimensions

Table 9.3. Tape and Reel Box Dimensions

Symbol	Dimensions [mm]
W_2	368
W_3	338
W_4	72

9.5 Moisture Sensitivity Level

Reels are delivered in packing which conforms to MSL3 (Moisture Sensitivity Level 3) requirements.

10. Soldering Recommendations

10.1 Soldering Recommendations

The BGM11S is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven, and particular type of solder paste used.

- Refer to technical documentations of particular solder paste for profile configurations.
- Avoid usining more than two reflow cycles.
- A no-clean, type-3 solder paste is recommended.
- A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- Recommended stencil thickness is 0.100 mm (4 mils).
- General SMT application notes are provided in AN1223.
- For further recommendation, refer to the JEDEC/IPC J-STD-020, IPC-SM-782 and IPC 7351 guidelines.
- The above notes are recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.

11. Certifications

Refer to AN1048 for information related to Regulatory Certifications.

11.1 Bluetooth Qualification

The BGM11S modules come with a pre-qualified Bluetooth Low Energy RF-PHY tested Component having Declaration ID of U049546 and QDID of 145424. This Component should be combined with the latest Wireless Gecko Link Layer and Host pre-qualified Components when in the process of qualifying the end-product via the SIG's Launch Studio.

11.2 CE and UKCA - EU and UK

The BGM11S modules have been tested against the relevant harmonized/designated standards and are in conformity with the essential requirements and other relevant requirements of the EU's Radio Equipment Directive (RED) (2014/53/EU) and of the UK's Radio Equipment Regulations (RER) (S.I. 2017/1206).

Please notice that every end-product integrating a BGM11S module will need to perform the radio EMC tests on the whole assembly, according to the ETSI 301 489-x relevant standards.

Furthermore, it is ultimately the responsibility of the manufacturers to ensure the compliance of their end-products as a whole. The specific product assembly is likely to have an impact to RF radiated characteristics, when compared to the bare module. Hence, manufacturers should carefully consider RF radiated testing with the final product assembly, especially taking into account the gain of the external antenna if any, and the possible deviations in the PSD, EIRP and spurious emissions measurements, as defined in the ETSI EN 300 328 standard.

The modules are entitled to carry the CE and UKCA Marks, and a formal Declaration of Conformity (DoC) is available at the product web page which is reachable starting from https://www.silabs.com/.

11.3 FCC

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesirable operation.

Any changes or modifications not expressly approved by Silicon Labs could void the user's authority to operate the equipment.

FCC RF Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure compliance. This transmitter meets both portable and mobile limits as demonstrated in the RF Exposure Analysis and SAR test report. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

OEM Responsibilities to comply with FCC Regulations:

The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

OEM integrator is responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

Important Note:

In the event that the above conditions cannot be met (for certain configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

The BGM11S Bluetooth module is labeled with its own FCC ID. If the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

"Contains Transmitter Module FCC ID: QOQ11"

Or

"Contains FCC ID: QOQ11"

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

11.4 ISED Canada

ISED Canada

This radio transmitter (IC: 5123A-11) has been approved by Industry Canada to operate with the embedded chip antenna. Other antenna types are strictly prohibited for use with this device.

This device complies with Industry Canada's license-exempt RSS standards. Operation is subject to the following two conditions:

1. This device may not cause interference; and
2. This device must accept any interference, including interference that may cause undesired operation of the device

RF Exposure Statement

BGM11S modules has been tested for worst case RF exposure. As demonstrated in the SAR test report,BGM11S can be mounted in touch with human body without further SAR evaluation.

OEM Responsibilities to comply with IC Regulations

The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

OEM integrator is responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

Important note

In the event that these conditions cannot be met (for certain configurations or co-location with another transmitter), then the IC authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate IC authorization

End Product Labeling

The BGM11S module is labeled with its own IC ID. If the IC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

"**Contains Transmitter Module IC: 5123A-11** "

or

"**Contains IC: 5123A-11"**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product

ISEDC (Français)

ISED Canada (Français)

Industry Canada a approuvé l'utilisation de cet émetteur radio (IC : 5123A-11) avec son antenne intégrée. L'utilisation de tout autre type d'antenne avec ce composant est proscrite.

Ce composant est conforme aux normes RSS, exonérées de licence d'Industry Canada. Son mode de fonctionnement est soumis aux deux conditions suivantes:

1. Ce composant ne doit pas générer d'interférences.
2. Ce composant doit pouvoir être soumis à tout type de perturbation y compris celle pouvant nuire à son bon fonctionnement.

Déclaration d'exposition RF

Les modules BGM11S ont été testés pour une exposition RF pire case. Comme indiqué dans le rapport de test DAS, BGM11S peut être assemblé en contact avec le corps humain sans évaluation DAS supplémentaire.

Responsabilités des OEM pour une mise en conformité avec le Règlement du Circuit Intégré

Le module émetteur ne doit pas être localisé ou fonctionner avec un autre émetteur ou une autre antenne que celle indiquée plus haut. Il incombe à l'intégrateur OEM de s'assurer de la bonne conformité du produit fini avec les autres normes auxquelles il pourrait être soumis de fait de l'utilisation de ce module (par exemple, les émissions des périphériques numériques, les exigences de périphériques PC, etc.).

Remarque Importante

Dans le cas où ces conditions ne peuvent être satisfaites (pour certaines configurations ou co-implantation avec un autre émetteur), l'autorisation IC n'est plus considérée comme valide et le numéro d'identification ID IC ne peut pas être apposé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera responsable de la réévaluation du produit final (y compris le module émetteur) et de l'obtention d'une autorisation IC distincte.

Étiquetage des produits finis

Le module BGM11S est étiqueté avec sa propre ID IC. Si l'ID IC n'est pas visible lorsque le module est intégré au sein d'un autre produit, cet autre produit dans lequel le module est installé devra porter une étiquette faisant apparaitre la référence du module intégré. Dans un tel cas, sur le produit final doit se trouver une étiquette aisément lisible sur laquelle figurent les informations suivantes:

"Contient le module transmetteur IC: 5123A-11"

ou

"Contient le circuit IC : 5123A-11"

L'intégrateur OEM doit être conscient qu'il ne doit pas fournir, dans le manuel d'utilisation, d'informations relatives à la façon d'installer ou de d'enlever ce module RF ainsi que sur la procédure à suivre pour modifier les paramètres liés à la radio.

11.5 Japan

The BGM11S is certified in Japan with certification number 209-J00255.

Important

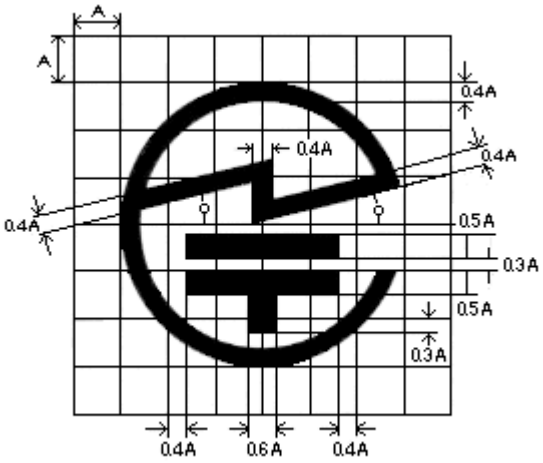
The module does is not labeled with Japan certification mark and ID because of the small physical size. Manufacturer who integrates a radio module in their host equipment must place the certification mark and certification number on the outside of the host equipment.

The certification mark and certification number must be placed close to the text in the Japanese language which is provided below.

当該機器には電波法に基づく、技術基準適合証明等を受けた特定無線設備を装着している。

Translation:

“This equipment contains specified radio equipment that has been certified to the Technical Regulation Conformity Certification under the Radio Law.”



11.6 KC South-Korea

BGM11S has certification in South-Korea.

Certification number: MSIP-CRM-BGT-BGM11S

11.7 NCC Taiwan

The BGM11S is certified in Taiwan with NCC certification number CCAM19LP0461T0 for BGM11S12A and CCAM19LP0460T1 for BGM11S22A.

BGM11S通过了台湾NCC认证, BGM11S12A认证号为CCAM19LP0461T0, BGM11S22A认证号为 CCAM19LP0460T1

The platform manufacturer is required to mark the platform with the following sentences:

- If using BGM11S12A: "This product contains an RF module with ID number CCAM19LP0461T0."
- If using BGM11S22A: "This product contains an RF module with ID number CCAM19LP0460T1."

平台制造商必须在平台上指定:

- 如果使用BGM11S12A: “本产品包含一个ID号为CCAM19LP0461T0的RF模块.”
- 如果使用BGM11S22A: “本产品包含一个ID号为CCAM19LP0460T1的RF模块.”

According to NCC Low Power Radio Wave Radiation Equipment Management Regulations:	
Article 12	A low-power RF equipment that has passed the type approval shall not change the frequency, increase the power or change the characteristics and functions of the original design without permission.
Article 14	The use of low-power RF equipment shall not affect flight safety and interfere with legal communications; if interference is found, it shall be immediately deactivated and improved until no interference is found. Legal communication in the preceding paragraph refers to radio communications operating in accordance with the provisions of the Telecommunications Act. Low-power RF equipment must withstand interference from legitimate communications or radiological, radiated electrical equipment for industrial, scientific, and medical applications.

根據 NCC 低功率電波輻射性電機管理辦法 規定:	
第十二條	經型式認證合格之低功率射頻電機，非經許可，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。
第十四條	低功率射頻電機之使用不得影響飛航安全及干擾合法通信；經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。 前項合法通信，指依電信法規定作業之無線電通信。 低功率射頻電機須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。

12. Revision History

Revision 1.4

October, 2022

- In the front page block diagram, updated the lowest energy mode for LETIMER.
- Updated 3.6.3 Low Energy Timer (LETIMER) lowest energy mode.
- Removed BIASPROG = 1, FULLBIAS = 0 specifications from 4.1.15 Analog Comparator (ACMP).
- Added timing specifications for RESETn low time and clarified V_{IL} and V_{IH} logic levels for RESETn pins in Table 4.20 GPIO on page 31.
- Added Figure 4.2 SPI Master Timing Diagram (SMSDELAY = 1) on page 43.
- Added a note about V_1V8 pin to 5.1 Typical Connections.
- Updated 11.2 CE and UKCA - EU and UK.
- Removed all references to RFSENSE.

Revision 1.3

April 2020

- Added reference to AN1223 and updated 10.1 Soldering Recommendations section.
- Added reference to AN1048 in 11. Certifications section.
- Updated 11.1 Bluetooth Qualification section with the new Declaration ID and QDID.

Revision 1.2

September 2019

- Added the SoC Family in the front page description.
- Updated Supported Protocol to Bluetooth® Low Energy in 1. Feature List.
- Updated the Protocol Stack in Table 2.1 Ordering Information on page 3 to Bluetooth® Low Energy.
- Replaced Bluetooth® Smart with Bluetooth® Low Energy wherever applicable.
- Removed Wake On Radio references wherever applicable since this feature is not supported by the software.
- Corrected the $RSSI_{MIN}$ and $RSSI_{MAX}$ specifications in 4.1.8.3 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band.
- Corrected the max Gain error in ADC in Table 4.22 ADC on page 33.
- Corrected the footprint in Figure 6.2 BGM11S PCB Middle and Bottom Layer Design on page 47.
- Updated Figure 7.2 BGM11S APORT on page 71 to clarify the APORT Connection Diagram.
- Divided the APORT table into individual tables based on Analog Peripherals in 7.3 Analog Port (APORT).
- Updated package markings with KC certification ID seen in 11.6 KC South-Korea in Figure 8.2 BGM11S Package Marking on page 78 .
- Updated Figure 8.3 Module Footprint on page 79 and Table 8.3 PCB Land Pattern Dimensions on page 79.
- Added a Note in Table 8.3 PCB Land Pattern Dimensions on page 79 regarding the differences in dimensions between the PCB Land Pattern (LPD) and Package Outline Drawing (POD).
- Added a Note in Table 8.3 PCB Land Pattern Dimensions on page 79 with general guidelines for users.
- Added a legend to and updated the Example Stencil Design in Figure 8.4 BGM11S Recommended Land Pattern on page 81
- Updated the certification information in 11.1 Bluetooth Qualification.
- Updated the French certification text in 11.4 ISED Canada.
- Updated section title and certification number in 11.6 KC South-Korea.
- Added certification number in 11.7 NCC Taiwan .

Revision 1.1

October 27th, 2017

- b and L dimensions adjusted in the PCB land pattern dimensions
- Maximum TX power for BGM11S12F256GA is amended to +2 dBm, was +3 dBm in earlier data sheet revisions
- ISED Canada certification added to front page certification list
- Power block (Figure 3.2) updated
- Typo in Figure 5.1 title text corrected
- Typo (2 of) corrected in first sentence of Section 5.1
- ISEDC changed to ISEC Canada in Section 11.4

Revision 1.0

- Pins 26 and 28 swapped in BGM11S pinout figure
- Layout guidelines updated
- Package specifications updated
- Package marking updated
- Soldering recommendations updated
- 1.0 data sheet for full production

Revision 0.91

- Layout guidelines updated
- Package specifications updated
- Package marking updated

Revision 0.90

- Preliminary version

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